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(54) SOLID-STATE IMAGE PICKUP DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a solid-state image pickup device capable of preventing the fluctuation of the loads of a vertical shift register for read and the vertical shift register for an electronic shutter in the case of performing an electronic shutter operation and preventing the generation of image noise such as horizontal stripes on the display screen of output signals.

SOLUTION: This device is provided with an image pickup area where a unit cell provided with a photodiode PD to be a pixel is two-dimensionally arranged, plural read lines 4 for driving the read transistor Td of each pixel row, plural vertical selection lines 6 for driving the vertical selection transistor Ta of each of the pixel rows, a vertical driving circuit 24 for selectively driving the plural read lines 4 and selectively driving the plural vertical selection lines 6, plural vertical signal lines VLIN for outputting signals from each unit cell of the successively driven pixel rows and row selection circuits 2, 21 and 22 for controlling the vertical driving circuit so as to successively drive the read transistor Td of each pixel two times at a desired signal storage timing and a signal read timing and to drive the vertical selection transistor Ta of the pixel row at the signal read timing.

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CLAIMS

[Claim(s)]

[Claim 1] A photo-electric-conversion means to carry out photo electric conversion of the incident light to a pixel, and to accumulate a charge, the read-out means which reads the accumulated charge to a detecting element, It comes to arrange the unit cell which has the perpendicular selection means to which a signal is made to output from the resetting means and said magnification means for resetting the charge of a magnification means to amplify the read charge, and said detecting element on a semi-conductor substrate two-

dimensional. The image pick-up field which has a pixel line for two or more signal read-out, and at least two dummy pixel lines, Two or more read lines for transmitting the read-out driving signal for driving each read-out means of the unit cell of a pixel line which is horizontally prepared corresponding to each pixel line in said image pick-up field, and corresponds, respectively, Two or more perpendicular selection lines for transmitting the line selection driving signal for driving each perpendicular selection means of the unit cell of a pixel line which is horizontally prepared corresponding to each pixel line in said image pick-up field, and corresponds, respectively, said -- more than one are read to the read line of a book, a driving signal is supplied alternatively, and said read-out means is driven -- both with the vertical-drive means for [said] supplying alternatively two or more line selection driving signals to the perpendicular selection line of a book, and driving said perpendicular selection means A line selection means to control said vertical-drive means to make the read-out means of each pixel line in said image pick-up field drive twice one by one to desired signal are recording timing and signal read-out timing, It is prepared corresponding to each pixel train in said image pick-up field, and two or more perpendicular signal lines for transmitting perpendicularly the signal outputted, respectively from each unit cell of the pixel line by which the sequential drive was carried out with said vertical-drive means are provided. After said line selection means controls signal read-out from the unit cell of the pixel line for said two or more signal read-out by said vertical-drive means, A selection control is carried out so that the 1st dummy pixel line of said two dummy pixel lines may be made to drive. The solid state camera characterized by carrying out a selection control so that the 2nd dummy pixel line of said said two dummy pixel lines may be made to drive after controlling the signal are recording in the unit cell of the pixel line for said two or more signal read-out by said vertical-drive means.

[Claim 2] In a solid state camera according to claim 1 said line selection means The shift register for the electronic shutters for controlling the initiation period of the signal are recording in said unit cell, It has a shift register for read-out for controlling the initiation period of signal read-out from said unit cell. Said 1st dummy pixel line It is the solid state camera which a selection control is carried out with the shift register for said read-out, and is characterized by carrying out the selection control of said 2nd dummy pixel line with the shift register for said electronic shutters.

[Claim 3] A photo-electric-conversion means to carry out photo electric conversion of the incident light to a pixel, and to accumulate a charge, the read-out means which reads the accumulated charge to a detecting element, It comes to arrange the unit cell which has the perpendicular selection means to which a signal is made to output from the resetting means and said magnification means for resetting the charge of a magnification means to amplify the read charge, and said detecting element on a semi-conductor substrate two-dimensional. Corresponding to each pixel line in the image pick-up field which has two or more pixel lines, and said image pick-up field, it is prepared horizontally. Two or more read lines for transmitting the read-out driving signal for driving each read-out means of the unit cell of a pixel line which corresponds, respectively, Two or more perpendicular selection lines for transmitting the line selection driving signal for driving each perpendicular selection means of the unit cell of a pixel line which is horizontally prepared corresponding to each pixel line in said image pick-up field, and corresponds, respectively, said -- more than one are read to the read line of a book, a driving signal is

supplied alternatively, and said read-out means is driven -- both with the vertical-drive means for [said] supplying alternatively two or more line selection driving signals to the perpendicular selection line of a book, and driving said perpendicular selection means A line selection means to control said vertical-drive means to make the read-out means of each pixel line in said image pick-up field drive twice one by one to desired signal are recording timing and signal read-out timing, It is prepared corresponding to each pixel train in said image pick-up field, and two or more perpendicular signal lines for transmitting perpendicularly the signal outputted, respectively from each unit cell of the pixel line by which the sequential drive was carried out with said vertical-drive means are provided. 1st means by which said line selection means makes the read-out means of each of said pixel line drive to said signal read-out timing with said vertical-drive means, The solid state camera characterized by providing 2nd at least two means to make the read-out means of each of said pixel line drive to said signal are recording timing with said vertical-drive means.

[Claim 4] In a solid state camera according to claim 3 said image pick-up field At least three dummy pixel lines other than said two or more pixel lines for signal read-out are provided further. Said line selection means The solid state camera characterized by making one dummy pixel line in said dummy pixel line drive with said 1st means, and making other two dummy pixel lines in said dummy pixel line drive with said 2nd two means.

[Claim 5] It is the solid state camera characterized by changing the signal are recording timing within the period of 1 field period in 1 field unit on a solid state camera according to claim 3 or 4 and corresponding to the period of the signal read-out timing of each pixel line in said line selection means.

[Claim 6] It is the solid state camera characterized by for said 2nd at least two means changing relatively the signal are recording timing to said signal read-out timing mutually in a solid state camera according to claim 5, making said read-out means drive, and switching the control action of said vertical-drive means by said 2nd means by turns for every field.

[Claim 7] In a solid state camera according to claim 5 the 1st means of said line selection means The shift register for read-out for controlling the initiation period of signal read-out from said unit cell is provided. The 2nd means of said line selection means The initiation period of the signal are recording in said unit cell in the shift register for the 1st electronic shutter for controlling the initiation period of the signal are recording in said unit cell in the 1st field period and the 1st [said] field period, and the 2nd field period repeated by turns The solid state camera characterized by providing the shift register for the 2nd electronic shutter for controlling.

[Claim 8] It is the solid state camera characterized by controlling said vertical-drive means to make the same substantially the electrical potential difference of other wiring which adjoins said read line around said photo-electric-conversion means also with the time of said two drives in case said line selection means makes the read-out means of each pixel line in said image pick-up field drive twice in claim 1 thru/or the solid state camera of any one publication of seven .

[Claim 9] Other wiring which adjoins said read line in a solid state camera according to claim 8 is solid state cameras characterized by being said perpendicular selection line.

[Claim 10] When reading stored charge from the optoelectric transducer of the unit cell

arranged two-dimensional to the image pick-up field on a semi-conductor substrate, In the solid state camera which performs electronic shutter actuation to which the signal which was made to drive twice one by one to the signal are recording timing and signal read-out timing of a request of wiring which controls this read-out, and was read to said signal read-out timing is made to output The solid state camera characterized by making the same substantially the electrical potential difference of other wiring which adjoins wiring which controls said read-out and exists around said optoelectric transducer to said signal are recording timing and signal read-out timing.

[Claim 11] In claim 1 thru/or the solid state camera of any one publication of ten said unit cell One read-out transistor to which the end side was connected to the cathode side of the photodiode which is one piece by which touch-down potential is given to an anode side, and said one photodiode, it read to the gate and the line was connected, One magnification transistor by which the gate was connected to the other end side of said read-out transistor, and the perpendicular signal line was connected to the end side, One perpendicular selection transistor by which the end side was connected to the other end side of said magnification transistor, and the perpendicular selection line was connected to the gate, It connects between one power-source line connected to the other end side of said perpendicular selection transistor, and the gate of said magnification transistor and said power-source line. The solid state camera characterized by providing in the gate one reset transistor to which the reset line was connected, and said one photodiode corresponding to one pixel.

[Claim 12] The solid state camera characterized by to be at the each pixel's read-out time, and to make the same substantially the electrical potential difference of other wiring which adjoins wiring which controls this read-out and exists around said optoelectric transducer in case the unit cell of 2 pixels / 1 unit reads stored charge from the 2-pixel optoelectric transducer in the unit cell of said image pick-up field in the solid state camera which has the image pick-up field which it comes to arrange on a semi-conductor substrate two-dimensional, respectively.

[Claim 13] In claim 1 thru/or the solid state camera of any one publication of 12 said unit cell One one end each is connected to each anode side respectively corresponding to each cathode side of the photodiode which is two pieces to which touch-down potential is given, and said two photodiodes. Two read-out transistors to which two read lines were connected respectively corresponding to each gate, One magnification transistor by which the gate was connected common to each said two other end side of a read-out transistor, and the perpendicular signal line was connected to the end side, One perpendicular selection transistor by which the end side was connected to the other end side of said magnification transistor, and said perpendicular selection line was connected to the gate, It connects between one power-source line connected to the other end side of said perpendicular selection transistor, and the gate of said magnification transistor and said power-source line. The solid state camera characterized by providing in the gate one reset transistor to which the reset line was connected, and said two photodiodes corresponding to two pixels.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a solid state camera, especially is used for a video camera, an electronic still camera, etc. about the good transformation child shutter control circuit of a solid state camera, and a pixel signal read-out control circuit.

[0002]

[Description of the Prior Art] Drawing 12 shows the equal circuit of the CMOS solid state camera (magnification mold CMOS image sensors) of the conventional example 1 equipped with the readout circuitry which a pixel signal can read for every pixel.

[0003] In drawing 12 , the unit cell of 1 pixel (1 pixel) / 1 unit is arranged in the shape of [which is two dimensions] a matrix, and is formed in the cel field (image pick-up field).

[0004] Each unit cell consists of four transistors Ta, Tb, Tc, and Td and one photodiode PD.

[0005] Namely, the photodiode PD with which touch-down potential is given to an anode side The read-out transistor Td by which the end side is connected to the cathode side of Photodiode PD (shutter gate transistor), The magnification transistor Tb by which the gate is connected to the other end side of the read-out transistor Td The reset transistor Tc by which the end side is connected to the gate of the perpendicular selection transistor (line selection transistor) Ta and the magnification transistor Tb where the end side is connected to the end side of the magnification transistor Tb is provided.

[0006] And corresponding to each pixel line, the perpendicular selection [which was connected common to the gate of each read-out transistor Td of the unit cell of the same line] line 6 connected with the line 4 common to the gate of each perpendicular selection transistor Ta of the unit cell of the same line and the reset line 7 connected common to the gate of each reset transistor Tc of the unit cell of the same line are formed in said cel field by reading.

[0007] Moreover, corresponding to each pixel train, the power-source line 9 connected common to the other end [of each reset transistor Tc of the unit cell of the same train as the perpendicular signal line VLIN connected common to the other end side of each magnification transistor Tb of the unit cell of the same train] and other end side of each perpendicular selection transistor Ta is formed in said cel field.

[0008] Furthermore, in the exterior by the side of the end of a cel field, two or more load transistors TL connected, respectively between one one end each of said perpendicular signal line VLIN and a touch-down node are arranged horizontally.

[0009] Moreover, in the exterior by the side of the other end of a cel field, two or more noise canceller circuits which consisted of two transistors TSH and TCLP and two capacitors Cc and Ct are arranged horizontally.

[0010] And two or more level selection transistors TH connected to each other end side of said perpendicular signal line VLIN through each above-mentioned noise canceller circuit are arranged horizontally.

[0011] The level signal line HLIN is connected to each other end of the above-mentioned level selection transistor TH in common, and they are a level reset transistor (not shown) and the output amplifying circuit AMP in this level signal line HLIN. It connects.

[0012] In addition, the transistor TSH for sample hold by which, as for said each noise canceller circuit, the end side was connected to the other end side of the perpendicular signal line VLIN Coupling-capacitor Cc by which the end side was connected to the other

end side of the transistor TSH for these sample hold, The capacitor Ct for charge storages connected between touch-down nodes the other end side of this coupling-capacitor Cc, It is constituted by the transistor TCLP for a potential clamp connected to the connection node of said capacitors Cc and Ct, and the end side of said level selection transistor TH is connected to the connection node of said capacitors Cc and Ct.

[0013] furthermore, in the exterior of a cel field Two or more perpendicular selection lines 6 of a cel field The timing generating circuit 10 which generates various kinds of timing signals for supplying the perpendicular shift register 2 for carrying out a selection control in scan, and said level selection transistor TH to the level shift register 3 for driving in scan, said noise canceller circuit, etc., The bias generating circuit 11 for generating predetermined bias potential at the end of the transistor TCLP for the potential clamp of said noise canceller circuit etc., Pulse selector 2a for carrying out the selection control of the output pulse of the above-mentioned perpendicular shift register 2, and driving the perpendicular selection line 6 of each line of a cel field in scan is arranged, respectively.

[0014] Drawing 13 is the timing wave form chart showing an example of actuation of the solid-state image sensors shown in drawing 12 .

[0015] Next, actuation of the solid-state image sensors of drawing 12 is explained, referring to drawing 13 .

[0016] The signal charge which photo electric conversion of the incident light of each photodiode PD was carried out, and it produced is accumulated into Photodiode PD.

[0017] In a horizontal blanking interval, in case the signal charge of Photodiode PD is read from the unit cell for a certain party, in order to choose each perpendicular signal line VLIN, the line selection transistor Ta for a party is first turned ON by turning ON the signal (phiADRES pulse) of the perpendicular selection line 6 of the line for selection.

[0018] The source follower circuit which consists of a magnification transistor Tb to which the power-source potential VDD (for example, 3.3V) is supplied through the line selection transistor Ta, and a load transistor TL in the unit cell for said party by this is operated.

[0019] Next, in the unit cell for said party, reference voltage is outputted to the perpendicular signal line VLIN by turning ON the signal (phiRESET pulse) of the reset line 7, and carrying out fixed period reset of the gate voltage of the magnification transistor Tb at reference voltage.

[0020] However, as described above, dispersion exists in the gate potential of the reset magnification transistor Tb, and dispersion appears also in the reset potential of the perpendicular signal line VLIN by the side of the other end.

[0021] Then, in order to reset dispersion in the reset potential of each perpendicular signal line VLIN The driving signal (phiSH pulse) of the transistor TSH for sample hold in a noise canceller circuit is turned ON beforehand (for example, the aforementioned phiADRES to ON and coincidence of a pulse). After reference voltage is outputted to said perpendicular signal line VLIN, by making the driving signal (phiCLP pulse) of the transistor TCLP for a potential clamp fixed time amount ON, reference voltage is set as the connection node of the capacitors Cc and Ct of a noise canceller circuit.

[0022] Next, aforementioned phiRESET After turning off a pulse, by choosing the read line 4 of a predetermined line and turning on the signal (phiREAD pulse), the read-out transistor Td is turned ON and gate potential is changed by reading the stored charge of

Photodiode PD to the gate of the magnification transistor Tb. The magnification transistor Tb outputs the voltage signal according to the variation of gate potential to the corresponding perpendicular signal line VLIN and a noise canceller circuit.

[0023] Then, a level effective scan term period can also accumulate the signal component (signal level from which the noise was removed) equivalent to the difference of the reference voltage read as described above, and a signal level in the capacitor Ct for charge storages by turning off phiSH pulse in a noise canceller circuit.

[0024] That is, the noise mixed in the preceding paragraph side from noise canceller circuits, such as dispersion in the reset potential of each perpendicular signal line VLIN resulting from a cel field, is removed.

[0025] And phiADRES By the perpendicular selection transistor's Ta being controlled by the OFF state, and changing a unit cell into the condition of not choosing, a cel field and each noise canceller circuit are electrically separated by turning OFF a pulse.

[0026] By making sequential ON the driving signal (phiH pulse) of the level selection transistor TH at a next horizontal effective scan period, the level selection transistor TH is turned on [sequential], the signal level of the connection node (signal preservation node) of said capacitors Cc and Ct is read to the level signal line HLIN one by one, and it is the output amplifying circuit AMP. It is amplified and outputs.

[0027] It sets in the above-mentioned actuation and is the electrical potential difference VVLIN of the perpendicular signal line VLIN. Noise rejection actuation which becomes the operating voltage Vm (about 1.5 V) of a source follower circuit and which was described in addition above is performed for every read-out actuation for every horizontal line at a horizontal blanking interval.

[0028] Drawing 14 is the timing wave form chart showing the timing generating circuit 10 in drawing 13 , the perpendicular shift register 2, and the example of pulse selector 2a of operation.

[0029] Here, the case where the solid state camera of drawing 12 is used by 1 field =1 / 30Hz (image of 30 frames per second which make the 1 field one frame) system is shown.

[0030] The timing generating circuit 10 operates external input pulse signal phiVR and phiHP orthopedically in a buffer circuit, and is pulse signal phiVRR of a field period. Pulse signal phiHPV of a level period It inputs into said perpendicular shift register 2.

[0031] The perpendicular shift register 2 is pulse signal phiVRR. Pulse signal phiHPV after an input clears all register outputs at the period of "L" level and makes it "L" level A shift action is performed, and the output pulse signal ROi (i=--, n, n+1, --) is made into "H" level one by one, and is inputted into said pulse selector 2a.

[0032] Pulse selector 2a activates the signal (phiADRES pulse) of the perpendicular selection line 6, the signal (phiRESET pulse) of the reset line 7, and the signal (phiREAD pulse) of the read line 4, as shown in drawing 13 to each line for selection, and it scans the line for selection.

[0033] It is each output pulse signal ROi of the perpendicular shift register 2 for the solid state camera of drawing 12 to carry out the selection control of the specific line for selection, as described above. It outputs only once within 1 field period. That is, since Photodiode PD performs signal read-out in the 1 field only once, the electronic shutter actuation which controls light-receiving time amount equivalent is impossible by controlling the signal storage time of Photodiode PD.

[0034] On the other hand, drawing 15 shows roughly the configuration of the CMOS solid state camera of the conventional example 2 in which electronic shutter actuation is possible.

[0035] This solid state camera For example, the image pick-up field 14 where the pixel cel 13 constituted as shown in drawing 12 has been arranged two-dimensional in the shape of a matrix (photo-electric-conversion section), Two or more perpendicular signal lines VLIN formed in the direction of a pixel train of said image pick-up field 14 Two or more perpendicular selection lines 6 for read-out control for controlling to be formed in the pixel line writing direction of said image pick-up field 14, and to read the photo-electric-conversion signal of each pixel cel 13 to said two or more perpendicular signal lines VLIN per pixel line, The 1st perpendicular selection circuitry 2 for carrying out a selection control in scan to the timing of read-out of said two or more perpendicular selection lines 6 for read-out control (perpendicular shift register for read-out), The level selection transistor TH for choosing said perpendicular signal line VLIN, The level selection circuitry 3 for carrying out the selection control of said level selection transistor (level selection shift register), Output amplifying circuit AMP for outputting the signal read to the level signal line HLIN and said level signal line HLIN for reading the signal of said perpendicular signal line VLIN chosen with said level selection shift register 3 It provides.

[0036] In addition, especially the point equipped with a load transistor as shown in drawing 12 , a noise canceller circuit, etc. around the image pick-up field 14 although not illustrated is the same as that of the CMOS solid state camera of an example 1.

[0037] Furthermore, the vertical-drive circuit (not shown) which generates the driving signal for driving alternatively said two or more perpendicular selection lines 6 for read-out control based on the output of the 2nd perpendicular selection circuitry (perpendicular shift register for electronic shutters) 15 for carrying out a selection control in scan and said 1st perpendicular selection circuitry and the output of the 2nd perpendicular selection circuitry to the timing of signal are recording of said two or more perpendicular selection lines 6 for read-out control is provided.

[0038] That is, the perpendicular shift register 15 for electronic shutters is formed independently [the perpendicular shift register 2 for read-out], and it is constituted so that this perpendicular shift register 15 for electronic shutters as well as the perpendicular shift register 2 for read-out may scan the line for selection to predetermined timing.

[0039] Thereby, the perpendicular shift register 2 for read-out and the perpendicular shift register 15 for electronic shutters enable it to carry out the selection control of the specific line for selection to 2 times of timing within 1 field period.

[0040] Therefore, when the perpendicular shift register 15 for electronic shutters carries out the selection control of the line for selection and starts are recording of a pixel signal before the twist from which the perpendicular shift register 2 for read-out carries out the selection control of the line for selection, and reads a pixel signal to the perpendicular signal line VLIN, the electronic shutter actuation which controls light-receiving time amount equivalent is attained.

[0041] By the way, the CMOS solid state camera of drawing 15 which has one perpendicular shift register 2 for read-out and one perpendicular shift register 15 for electronic shutters which were described above For example, when making the good transformation child shutter actuation to which light-receiving time amount is changed

equivalent by changing the signal storage time automatically according to the output level of a photo sensor perform There is a problem of the difference of the signal storage time arising to pixel spacing, or changing the load of two perpendicular shift registers 2 and 15 to it according to the merits and demerits of the signal storage time.

[0042] This problem is explained below.

[0043] Drawing 16 shows an example in case the line selection timing of two perpendicular shift registers 2 and 15 in drawing 15 is immobilization.

[0044] As shown in drawing 16 , the timing to which the perpendicular shift register 15 for electronic shutters performs line selection ahead of the perpendicular shift register 2 for read-out is being fixed, that is, the two above-mentioned perpendicular shift registers 2 and 15 of the time difference which performs line selection are always fixed.

[0045] Thus, when the line selection timing of two perpendicular shift registers 2 and 15 is immobilization, the perpendicular shift register 2 for read-out and the perpendicular shift register 15 for electronic shutters begin selection of return and the following frame to the first rank again, after it begins selection of a certain frame and the shift action from the first rank to a tail end (that is, the number of pixels of the perpendicular direction of a solid state camera) finishes.

[0046] Therefore, the solid state camera of drawing 15 has the problem of the difference of the signal storage time arising to pixel spacing, or changing the load of two perpendicular shift registers 2 and 15 to it according to the merits and demerits of the signal storage time, when making the good transformation child shutter actuation to which light-receiving time amount is changed equivalent by changing the signal storage time automatically according to the output level of a photo sensor perform.

[0047] Here, said problem is stated to a detail, referring to drawing 17 about the case where the merits and demerits of the time amount in which the perpendicular shift register 15 for electronic shutters changes the timing (timing of an electronic shutter) which performs line selection ahead of the perpendicular shift register 2 for read-out, and accumulates a pixel signal as concrete technique for changing the signal storage time are changed.

[0048] In drawing 17 , a read-out control pulse is a signal which makes the shift action of the perpendicular shift register 2 for read-out start, and a good transformation child shutter control pulse is a signal which makes the shift action of the perpendicular shift register 15 for electronic shutters start.

[0049] (1) After starting the shift action of the perpendicular shift register 15 for electronic shutters by the control pulse of the electronic shutter generated to the timing t1 in drawing 17 on the occasion of selection of the 1st frame, before the shift action to a tail end finishes (before choosing all pixel lines), in order to choose the 2nd frame to the timing t3 in drawing 17 , suppose that the electronic shutter pulse occurred. In this case, the perpendicular shift register 15 for electronic shutters is reset to the above-mentioned timing t3, and starts a shift action (line selection) from the first rank again.

[0050] Thereby, in case [at which it generated to the timing t2 in drawing 17] it reads, and the shift action of the perpendicular shift register 2 for read-out begins by the control pulse and said 1st frame is read, the difference of the signal storage time arises in the pixel line by which selection assignment was not carried out with the pixel line by which selection assignment was carried out with the perpendicular shift register 15 for electronic shutters which the shift action started to said timing t1.

[0051] Thus, if the difference of the signal storage time arises, when a read-out output level is changed depending on the location of a pixel line and displays the output signal of a solid state camera on the screen of an image display device, it will become the cause which image noises, such as a lateral stripe, generate.
[0052] (2) in the timing t4 in drawing 17 , the shift action began to the selection line and said timing t2 of the perpendicular shift register 15 for electronic shutters which the shift action started to said timing t3 -- reading -- business -- since a total of two pixel lines of the selection line of the perpendicular shift register 2 are chosen, these two pixel lines serve as a load of two perpendicular shift registers 2 and 15.
[0053] on the other hand, in the timing t6 in drawing 17 , the selection line by the perpendicular shift register 15 for electronic shutters which the shift action started to said timing t3 did not already exist, but the shift action started it to the timing t5 in drawing 17 -- reading -- business -- since one pixel line is chosen with the perpendicular shift register 2, this one pixel line serves as a load of two perpendicular shift registers 2 and 15.
[0054] Thus, if the load of two perpendicular shift registers 2 and 15 is changed depending on electronic shutter timing, the voltage variation of power-source Rhine of a solid state camera is imitated, and it comes, and when the output signal of a solid state camera is displayed on the screen of an image display device, a lateral stripe will be generated, and it will become the cause which worsens image quality notably.
[0055] In addition, the problem of the difference of the signal storage time arising to pixel spacing, or changing the load of two perpendicular shift registers 2 and 15 to it according to the merits and demerits of the signal storage time which was described above is produced not only the solid state camera of a CMOS mold but when making the solid state camera of a CCD mold perform good transformation child shutter actuation.
[0056]
[Problem(s) to be Solved by the Invention] As described above, when changing the signal storage time and making good transformation child shutter actuation perform, according to the merits and demerits of the signal storage time, the difference of the signal storage time arose to pixel spacing, or the load of the perpendicular shift register for read-out and the perpendicular shift register for electronic shutters was changed, and the conventional solid state camera had the problem of becoming the cause which image noises, such as a lateral stripe, generate in the display screen of an output signal.
[0057] the case where it was made that this invention should solve the above-mentioned trouble, and electronic shutter actuation is made to perform -- reading -- business -- fluctuation of the load of a perpendicular shift register and the perpendicular shift register for electronic shutters can be prevented, and it aims at offering the solid state camera which can prevent generating of image noises, such as a lateral stripe in the display screen of an output signal.
[0058] moreover, the case where this invention makes the good transformation child shutter actuation (continuation electronic shutter actuation) to which the signal storage time of a pixel is changed per field perform -- reading -- business -- fluctuation of the load of a perpendicular shift register and the perpendicular shift register for electronic shutters can be prevented, and it aims at offering the solid state camera which can prevent generating of image noises, such as a lateral stripe in the display screen of an output signal.
[0059] Moreover, this invention aims at offering the solid state camera which can prevent

that the difference of the signal storage time arises to pixel spacing according to the merits and demerits of the signal storage time, when making continuation electronic shutter actuation perform.

[0060] Moreover, this invention aims at offering the solid state camera which can prevent generating of image noises, such as a lateral stripe in the display screen of an output signal, when making continuation electronic shutter actuation perform.

[0061] Moreover, in case this invention reads photo electric conversion and the accumulated signal by the pixel, it aims at offering the solid state camera which can prevent that a noise jumps in by capacity coupling from wiring of the pixel circumference.

[0062]

[Means for Solving the Problem] A photo-electric-conversion means for the 1st solid state camera of this invention to carry out photo electric conversion of the incident light to a pixel, and to accumulate a charge, The read-out means which reads the accumulated charge to a detecting element, a magnification means to amplify the read charge, It comes to arrange the unit cell which has the perpendicular selection means to which a signal is made to output from the resetting means and said magnification means for resetting the charge of said detecting element on a semi-conductor substrate two-dimensional. The image pick-up field which has a pixel line for two or more signal read-out, and at least two dummy pixel lines, Two or more read lines for transmitting the read-out driving signal for driving each read-out means of the unit cell of a pixel line which is horizontally prepared corresponding to each pixel line in said image pick-up field, and corresponds, respectively, Two or more perpendicular selection lines for transmitting the line selection driving signal for driving each perpendicular selection means of the unit cell of a pixel line which is horizontally prepared corresponding to each pixel line in said image pick-up field, and corresponds, respectively, said -- more than one are read to the read line of a book, a driving signal is supplied alternatively, and said read-out means is driven -- both with the vertical-drive means for [said] supplying alternatively two or more line selection driving signals to the perpendicular selection line of a book, and driving said perpendicular selection means A line selection means to control said vertical-drive means to make the read-out means of each pixel line in said image pick-up field drive twice one by one to desired signal are recording timing and signal read-out timing, It is prepared corresponding to each pixel train in said image pick-up field, and two or more perpendicular signal lines for transmitting perpendicularly the signal outputted, respectively from each unit cell of the pixel line by which the sequential drive was carried out with said vertical-drive means are provided. After said line selection means controls signal read-out from the unit cell of the pixel line for said two or more signal read-out by said vertical-drive means, A selection control is carried out so that the 1st dummy pixel line of said two dummy pixel lines may be made to drive. After controlling the signal are recording in the unit cell of the pixel line for said two or more signal read-out by said vertical-drive means, it is characterized by carrying out a selection control so that the 2nd dummy pixel line of said said two dummy pixel lines may be made to drive.

[0063] A photo-electric-conversion means for the 2nd solid state camera of this invention to carry out photo electric conversion of the incident light to a pixel, and to accumulate a charge, The read-out means which reads the accumulated charge to a detecting element, a magnification means to amplify the read charge, The image pick-up field which it comes

to arrange the unit cell which has the perpendicular selection means to which a signal is made to output from the resetting means and said magnification means for resetting the charge of said detecting element on a semi-conductor substrate two-dimensional, and has two or more pixel lines, Two or more read lines for transmitting the read-out driving signal for driving each read-out means of the unit cell of a pixel line which is horizontally prepared corresponding to each pixel line in said image pick-up field, and corresponds, respectively, Two or more perpendicular selection lines for transmitting the line selection driving signal for driving each perpendicular selection means of the unit cell of a pixel line which is horizontally prepared corresponding to each pixel line in said image pick-up field, and corresponds, respectively, said -- more than one are read to the read line of a book, a driving signal is supplied alternatively, and said read-out means is driven -- both with the vertical-drive means for [said] supplying alternatively two or more line selection driving signals to the perpendicular selection line of a book, and driving said perpendicular selection means A line selection means to control said vertical-drive means to make the read-out means of each pixel line in said image pick-up field drive twice one by one to desired signal are recording timing and signal read-out timing, It is prepared corresponding to each pixel train in said image pick-up field, and two or more perpendicular signal lines for transmitting perpendicularly the signal outputted, respectively from each unit cell of the pixel line by which the sequential drive was carried out with said vertical-drive means are provided. 1st means by which said line selection means makes the read-out means of each of said pixel line drive to said signal read-out timing with said vertical-drive means, It is characterized by providing 2nd at least two means to make the read-out means of each of said pixel line drive to said signal are recording timing with said vertical-drive means.

[0064] The 3rd solid state camera of this invention is set to said 2nd solid state camera. Said image pick-up field At least three dummy pixel lines other than said two or more pixel lines for signal read-out are provided further. Said line selection means It is characterized by making one dummy pixel line in said dummy pixel line drive with said 1st means, and making other two dummy pixel lines in said dummy pixel line drive with said 2nd two means.

[0065] It is characterized by the 4th solid state camera of this invention changing the signal are recording timing within the period of 1 field period in said 2nd or 3rd solid state camera in 1 field unit corresponding to the period of the signal read-out timing of each pixel line in said line selection means.

[0066] In said 4th solid state camera, said 2nd at least two means changes relatively the signal are recording timing to said signal read-out timing mutually, and makes said read-out means drive, and the 5th solid state camera of this invention is characterized by switching the control action of said vertical-drive means by said 2nd means by turns for every field.

[0067] The 6th solid state camera of this invention is characterized by said line selection means controlling said vertical-drive means to make the same substantially the electrical potential difference of other wiring which adjoins said read line around said photo-electric-conversion means also with the time of said two drives, in case the read-out means of each pixel line in said image pick-up field is made to drive twice in said any 1st thru/or 5th one solid state camera.

[0068] When the 7th solid state camera of this invention reads stored charge from the

optoelectric transducer of the unit cell arranged two-dimensional to the image pick-up field on a semi-conductor substrate, In the solid state camera which performs electronic shutter actuation to which the signal which was made to drive twice one by one to the signal are recording timing and signal read-out timing of a request of wiring which controls this read-out, and was read to said signal read-out timing is made to output Wiring which controls said read-out is adjoined and it is characterized by making the same substantially the electrical potential difference of other wiring which exists around said optoelectric transducer to said signal are recording timing and signal read-out timing.

[0069] In the solid state camera with which, as for the 8th solid state camera of this invention, the unit cell of 2 pixels / 1 unit has the image pick-up field which it comes to arrange on a semi-conductor substrate two-dimensional In case stored charge is read from the 2-pixel optoelectric transducer in the unit cell of said image pick-up field, respectively, wiring which controls this read-out is adjoined and it is characterized by making the same substantially the electrical potential difference of other wiring which exists around said optoelectric transducer at the time of read-out of each pixel.

[0070]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing.

[0071] <Gestalt of the 1st operation> drawing 1 shows the equal circuit of the magnification mold CMOS solid state camera of the gestalt of the 1st operation.

[0072] Although most is the same compared with the CMOS solid state camera of the conventional example 2 which mentioned above the CMOS solid state camera of drawing 1 with reference to drawing 15 , perpendicular shift register 2a for read-out differs from perpendicular shift register 15a for electronic shutters etc., and since others are the same, they attach the same sign as the inside of drawing 15 .

[0073] The CMOS solid state camera of drawing 1 Namely, for example, the image pick-up field 14 where the pixel cel 13 constituted as the conventional example 1 of drawing 12 showed has been arranged two-dimensional in the shape of a matrix (photo-electric-conversion section), Two or more perpendicular signal lines VLIN formed in the direction of a pixel train of said image pick-up field 14 Two or more perpendicular selection lines 6 for read-out control for controlling to be formed in the pixel line writing direction of said image pick-up field 14, and to read the photo-electric-conversion signal of each pixel cel 13 to said two or more perpendicular signal lines VLIN per pixel line, 1st perpendicular selection-circuitry (perpendicular shift register for read-out) 2a for carrying out a selection control in scan to the timing of read-out of said two or more perpendicular selection lines 6 for read-out control, 2nd perpendicular selection-circuitry (perpendicular shift register for electronic shutters) 15a for carrying out a selection control in scan to the timing of signal are recording of said two or more perpendicular selection lines 6 for read-out control, The vertical-drive circuit 16 which generates the driving signal for driving alternatively said two or more perpendicular selection lines 6 for read-out control based on the output of said 1st perpendicular selection-circuitry 2a, and the output of 2nd perpendicular selection-circuitry 15a (pulse selector), The level selection transistor TH for choosing said perpendicular signal line VLIN, The level selection circuitry 3 for carrying out the selection control of said level selection transistor TH (level selection shift register), Output amplifying circuit AMP for outputting the signal read to the level signal line HLIN and said level signal line HLIN for reading the

signal of said perpendicular signal line VLIN chosen with said level selection shift register 3 It provides.

[0074] In addition, like the CMOS solid state camera of the conventional example 2 of drawing 15 , although not illustrated especially here, it has a load transistor, a noise canceller circuit, etc. as shown in drawing 12 around the image pick-up field 14.

[0075] and -- further -- (1) -- apart from the original pixel line, two dummy pixel lines (the 1st dummy pixel line 141 and 2nd dummy pixel line 142) are added to said image pick-up field 14. (2) Perpendicular shift register (1st perpendicular shift register) 2a for said read-out has the shift number of stages of the original pixel line count +1 of the image pick-up field 14, and perpendicular shift register (2nd perpendicular shift register) 15a for said electronic shutters also has the shift number of stages of the original pixel line count +1 of the image pick-up field 14. (3) The vertical-drive circuit 16 is constituted so that the last stage output signal of perpendicular shift register 2a for read-out is chosen, said 1st dummy pixel line 141 may be supplied, the last stage output signal of perpendicular shift register 15a for electronic shutters may be chosen and said 2nd dummy pixel line 142 may be supplied.

[0076] Although it is the same configuration as an original pixel line, said two dummy pixel lines 141 and 142 are added in order to act as a load, when chosen by the vertical-drive circuit 16.

[0077] In the solid state camera of drawing 1 , shutter actuation which it is possible to carry out the selection control of the same perpendicular selection line twice within 1 field period, and controls the signal storage time of a pixel (photodiode) by perpendicular shift register 15a for electronic shutters and perpendicular shift register 2a for read-out can be performed.

[0078] in this case, perpendicular shift register 15a for electronic shutters performs a shift action based on the shift clock signal which controls the initiation timing of signal are recording, carries out the selection control of the pixel line which each corresponds to a shutter actuation period, and makes signal are recording of a pixel perform (read-out does not perform) -- it controls like and the selection control of the 2nd dummy pixel line 142 carries out except a shutter actuation period (the period from after the end of selection of a pixel line to next selection initiation).

[0079] Moreover, perpendicular shift register 2a for read-out performs a shift action based on the shift clock signal which controls the initiation timing of signal read-out, carries out the selection control of the pixel line which each corresponds to each level period in the perpendicular effective scan period within a perpendicular period, and carries out the selection control of the 1st dummy pixel line 141 to a vertical-retrace-line period.

[0080] According to the solid state camera of the gestalt of implementation of the above 1st, namely, the vertical-drive circuit 16 Respectively corresponding to each output of perpendicular shift register 2a for read-out, and perpendicular shift register 15a for electronic shutters, are always carrying out the selection drive of the pixel line per (a total of 2), and since the selection load is always equal Generating of the disk on the display screen resulting from fluctuation of the read-out level by the size of a selection load can be prevented.

[0081] <Gestalt of the 2nd operation> drawing 2 shows the equal circuit of the magnification mold CMOS solid state camera of the gestalt of the 2nd operation.

[0082] As opposed to the CMOS solid state camera of the gestalt of the 1st operation which mentioned above the CMOS solid state camera of drawing 2 with reference to drawing 1 (1) The point that one more dummy pixel line (3rd dummy pixel line 143) is added to said image pick-up field 14, (2) Perpendicular shift register 15b for one electronic shutters which has the same shift number of stages as perpendicular shift register 15a further for electronic shutters is added. The point which each of that stage output switches per each stage output of perpendicular shift register 15a for said electronic shutters, and field, is chosen, and is used by vertical-drive circuit (pulse selector) 16a, (3) Vertical-drive circuit 16a Three perpendicular shift registers 2a and 15a, Point and (4) vertical-drive circuits 16a which generates the driving signal for driving alternatively said two or more perpendicular selection lines 6 for read-out control based on the output of 15b The points which choose the last stage output signal of added perpendicular shift register 15b for electronic shutters, and are supplied to said 3rd dummy pixel line 143 differ a little, and since others are the same, they attach the same sign as the inside of drawing 1 .

[0083] Drawing 3 is the timing chart showing signs that two perpendicular shift registers 15a and 15b for electronic shutters control electronic shutter actuation by turns per field, in the solid state camera of drawing 2 .

[0084] In the solid state camera of drawing 2 , electronic shutter actuation is distributed to two perpendicular shift registers 15a and 15b only for electronic shutters in the field unit at alternation by making the shift action of two perpendicular shift registers 15a and 15b only for electronic shutters start by turns per field, and choosing each output by turns per field so that it may understand from the timing chart shown in drawing 3 .

[0085] In this case, the selected perpendicular shift registers 15a and 15b only for electronic shutters perform line selection ahead of perpendicular shift register 2a for read-out, and it becomes possible by changing that timing to change the merits and demerits of the time amount which accumulates a pixel signal.

[0086] Therefore, the same vertical lines can be chosen twice as 1 field period with the perpendicular shift registers 15a and 15b for electronic shutters, and the perpendicular shift register 2 for read-out, and good transformation child shutter actuation which controls the signal storage time of a selection pixel can be performed.

[0087] Moreover, without while having already started the shift action, and being reset on the way, before the shift action of the perpendicular shift registers 15a or 15b only for electronic shutters arrives at the last stage even if an electronic shutter control signal is inputted with a time interval shorter than a field period (before finishing no selection of the pixel lines for read-out), sequential selection is made to the last pixel line, and the signal storage time of a selection pixel is controlled.

[0088] And the period from after the end of selection of the last line of the pixel line for read-out to selection initiation [in / one after another / the field period of a time] of the pixel line for read-out of the 1st line carries out the selection control of the 2nd dummy pixel line 142 or the 3rd dummy pixel line 143.

[0089] Moreover, perpendicular shift register 2a for read-out carries out the selection control of the pixel line which each corresponds to each level period within a perpendicular effective scan period, and carries out the selection control of the 1st dummy pixel line 141 to a vertical-retrace-line period.

[0090] That is, each perpendicular shift registers 2a, 15a, and 15b continue choosing a

dummy pixel line, even after choosing the pixel line for all read-out, respectively, and they stand by the selection initiation in a next field period.

[0091] That is, according to the solid state camera of the gestalt of implementation of the above 2nd, it becomes possible in a field unit to change the signal storage time to two perpendicular shift registers only for electronic shutters between the fields by distributing electronic shutter actuation at alternation.

[0092] In this case, it becomes possible to realize electronic shutter ability to which the signal storage time is continuously changed per field, while the scan time of read-out has been fixed. In addition, in the same field, every selection pixel line of the signal storage time is the same.

[0093] Thus, when changing the signal storage time and making good transformation child shutter actuation perform, it can prevent that the difference of the signal storage time arises to pixel spacing according to the merits and demerits of the signal storage time, and generating of image noises, such as a lateral stripe in the display screen of an output signal, can be prevented.

[0094] Moreover, vertical-drive circuit 16a is always carrying out the selection drive of the pixel line per (a total of 3) respectively corresponding to each output of perpendicular shift register 2a for read-out, and the perpendicular shift registers 15a and 15b for two electronic shutters, and since the selection load is always equal, it can prevent generating of the disk on the display screen resulting from fluctuation of the read-out level by the size of a selection load.

[0095] In addition, the solid state camera shown in drawing 1 and drawing 2 is applicable not only to the solid state camera of the CMOS mold equipped with the readout circuitry which a pixel signal can read for every pixel but the solid state camera of the CCD (charge coupled devices) mold which reads in a level signal-line unit.

[0096] <Gestalt of the 3rd operation> drawing 4 shows the equal circuit of the magnification mold CMOS solid state camera of the gestalt of the 3rd operation.

[0097] When the CMOS solid state camera of drawing 4 changes the signal storage time automatically according to the output level of a photo sensor as opposed to the CMOS solid state camera of the conventional example 1 mentioned above with reference to drawing 12 , the device is made so that it may become possible to change continuously the good transformation child shutter actuation to which light-receiving time amount is changed equivalent per field.

[0098] Namely, although most is the same compared with the CMOS solid state camera of the conventional example 1 which mentioned above the CMOS solid state camera of drawing 4 with reference to drawing 12 (1) The point that two perpendicular shift registers 21 and 22 for electronic shutters are added independently [the perpendicular shift register 2 for read-out], (3) The point that the register change-over control circuit (SEL) 23 for switching actuation (output actuation of the control pulse of the signal storage time) of two perpendicular shift registers 21 and 22 for electronic shutters by turns per field, and controlling it is added, (4) The configurations of timing generating circuit 10a and the pulse selector circuit 24 differ, and since others are the same, they attach the same sign as the inside of drawing 12 .

[0099] That is, in drawing 4 , four transistors Ta, Tb, Tc, and Td and the unit cell of 1 pixel (1 pixel) / 1 unit which consists of one photodiode PD are arranged in the shape of [which is two dimensions] a matrix, and are formed in the cel field (image pick-up field).

In this case, the photodiode PD with which, as for each unit cell, touch-down potential is given to an anode side The read-out transistor Td by which the end side is connected to the cathode side of Photodiode PD (shutter gate transistor), The magnification transistor Tb by which the gate is connected to the other end side of the read-out transistor Td The reset transistor Tc by which the end side is connected to the gate of the perpendicular selection transistor (line selection transistor) Ta and the magnification transistor Tb where the end side is connected to the end side of the magnification transistor Tb is provided.

[0100] And two or more read lines 4 connected to said cel field corresponding to each pixel line common to the gate of each read-out transistor Td of the unit cell of the same line, the perpendicular selection line 6 connected common to the gate of each perpendicular selection transistor Ta of the unit cell of the same line, and the reset line 7 connected common to the gate of each reset transistor Tc of the unit cell of the same line are formed.

[0101] Moreover, corresponding to each pixel train, the power-source line 9 connected common to the other end [of each reset transistor Tc of the unit cell of the same train as the perpendicular signal line VLIN connected common to the other end side of each magnification transistor Tb of the unit cell of the same train] and other end side of each perpendicular selection transistor Ta is formed in said cel field.

[0102] Furthermore, in the exterior by the side of the end of a cel field, two or more load transistors TL connected, respectively between one one end each of said perpendicular signal line VLIN and a touch-down node are arranged horizontally.

[0103] Moreover, in the exterior by the side of the other end of a cel field, two or more noise canceller circuits which consisted of two transistors TSH and TCLP and two capacitors Cc and Ct are arranged horizontally.

[0104] And two or more level selection transistors TH connected to each other end side of said perpendicular signal line VLIN through each above-mentioned noise canceller circuit are arranged horizontally.

[0105] The level signal line HLIN is connected to each other end of the above-mentioned level selection transistor TH in common, and they are a level reset transistor (not shown) and the output amplifying circuit AMP in this level signal line HLIN. It connects.

[0106] In addition, the transistor TSH for sample hold by which, as for said each noise canceller circuit, the end side was connected to the other end side of the perpendicular signal line VLIN Coupling-capacitor Cc by which the end side was connected to the other end side of the transistor TSH for these sample hold, The capacitor Ct for charge storages connected between touch-down nodes the other end side of this coupling-capacitor Cc, It is constituted by the transistor TCLP for a potential clamp connected to the connection node of said capacitors Cc and Ct, and the end side of said level selection transistor TH is connected to the connection node of said capacitors Cc and Ct.

[0107] furthermore, in the exterior of a cel field The selection control of the output pulse of the perpendicular shift register 2 for read-out for carrying out the selection control of two or more perpendicular selection lines 6 of a cel field in scan, two perpendicular shift registers 21 and (ES2) 22 for electronic shutters (ES1), and the three above-mentioned perpendicular shift registers 2, 21, and 22 is carried out. The perpendicular selection line 6 of each line of a cel field Actuation (output actuation of the control pulse of the signal storage time) of the level shift register 3 for driving the pulse selector 24 for driving in

scan, and said two or more level selection transistors TH in scan, and said perpendicular shift registers 21 and 22 for two electronic shutters The register change-over control circuit 23 for switching by turns per field and controlling, timing generating circuit which generates various kinds of timing signals 10a, The bias generating circuit 11 for generating predetermined bias potential at the end of the transistor TCLP for the potential clamp of said noise canceller circuit etc. is arranged, respectively.

[0108] Timing signal phiVR of a field period, timing signal phiES for storage-time control by which an adjustable setup is carried out with a field period, pulse signal phiHP corresponding to a horizontal blanking interval, and clock pulse signal phiCK input said timing generating circuit 10a.

[0109] And timing signal phiVRR for carrying out buffer plastic surgery, reading said timing signal phiVR input, and supplying the perpendicular shift register of business is generated, and timing signal phiHPV for carrying out buffer plastic surgery, reading said pulse signal phiHP input, and supplying the perpendicular shift register of business and two perpendicular shift registers 21 and 22 for electronic shutters is generated.

[0110] Moreover, timing signal phiROREAD for supplying said pulse selector 24, phiESREAD, phiRESET, and phiADRES are generated, and pulse signal phiCLP for supplying said noise canceller circuit and phiSH are generated. Moreover, pulse signal phiH for supplying the level shift register 3 is generated.

[0111] Moreover, based on timing signal phiVR of a field period, pulse signal phiFI for field change-over control is generated, and said register change-over control circuit 23 is supplied with timing signal phiESR for signal storage-time control.

[0112] Said register change-over control circuit 23 switches the supply place of timing signal phiESR for storage-time control by turns for every field unit based on the pulse signal phiFI input for field change-over control. In this case, the timing signal for signal storage-time control which supplies the timing signal for signal storage-time control supplied to the perpendicular shift register 21 for said electronic shutters to phiESR1 and the perpendicular shift register 22 for said electronic shutters is expressed with phiESR2.

[0113] Drawing 5 is the circuit diagram showing an example of the pulse selector 24 in drawing 4 .

[0114] While each output-signal ES1n of the output signal ROn of the perpendicular shift register for read-out and two perpendicular shift registers 21 and 22 for electronic shutters and ES2n input the pulse selector shown in drawing 5 Timing signal phiROREAD supplied from said timing generating circuit 10a, phiESREAD, phiRESET, and phiADRES input, logic processing of these input signals is performed and various kinds of driving signal phiREADn(s), phiRESET, and phiADRESn are outputted, and it is constituted by the logic gate so that a cel field may be supplied.

[0115] That is, when the output signal ROn of the perpendicular shift register for read-out is an active state, timing signal phiROREAD is chosen and read and it outputs as line driving signal phiREADn, and when each output signal ES1n of two perpendicular shift registers 21 and 22 for electronic shutters or ES2n is an active state, timing signal phiESREAD is chosen and read and it outputs as line driving signal phiREADn.

[0116] Moreover, when any one of each output-signal ES1n of the output signal ROn of the perpendicular shift register for read-out and two perpendicular shift registers 21 and 22 for electronic shutters and the ES2n is an active state, timing signal phiRESET is chosen and it outputs as reset line driving signal phiRESETn.

[0117] Moreover, when the output signal ROn of the perpendicular shift register for read-out is an active state, timing signal phiADRES is chosen and it outputs as perpendicular selection line driving signal phiADRESn.

[0118] Drawing 6 is the timing wave form chart showing the example of timing generating circuit 10a in drawing 4 , three perpendicular shift registers 2, 21, and 22, and the pulse selector 24 of operation, in order to explain the good transformation child shutter actuation with possible making it change continuously in the field unit in the solid state camera of drawing 4 .

[0119] Here, the case where the solid state camera of drawing 4 is used by 1 field =1 / 30Hz (image of 30 frames per second which make the 1 field one frame) image pick-up system is shown.

[0120] The timing signal input for storage-time control by which an adjustable setup of the timing signal input of a field period and the phiES is carried out for phiVR with a field period in drawing 6 , The timing signal of a field period with which phiVRR is supplied to the perpendicular shift register for read-out, The pulse signal for field change-over control in phiFI, the timing signal for storage-time control with which phiESR1 is supplied to the perpendicular shift register 21 for one electronic shutters every other field, The timing signal for storage-time control with which phiESR2 is supplied to the perpendicular shift register 22 for the electronic shutters of another side at intervals of 1 field, R0 (i) is the output of the perpendicular shift register R0 for read-out, and ES1 (i). The output of the perpendicular shift register 21 for one electronic shutters, and ES2 (i) It is the output of the perpendicular shift register 22 for the electronic shutters of another side.

[0121] Drawing 7 is the timing wave form chart showing an example of the electronic shutter actuation within 1 field period in drawing 6 .

[0122] In drawing 7 , the perpendicular shift register 21 for electronic shutters in ESn or the n-th step of output signal of 22, and ROn are the n-th step of output signals of the perpendicular shift register 2 for read-out.

[0123] tHES shows 1 level period when the perpendicular shift register 21 for electronic shutters or the n-th step of output signal ESn of 22 will be in an active state ("H" level).

[0124] tHRO shows 1 level period when the n-th step of output signal ROn of the perpendicular shift register 2 for read-out will be in an active state ("H" level).

[0125] HBLK is a control pulse signal for dividing 1 level period into a horizontal blanking interval and a horizontal effective scan period.

[0126] phiCLP and phiSH are pulse signals supplied to a noise canceller circuit, and are generated for every horizontal blanking interval, respectively.

[0127] phiH is a pulse signal supplied to the level selection transistor TH, and it is generated so that the level selection transistor TH horizontally arranged within a level effective-scanning-lines period may be turned on [sequential].

[0128] Although phiADRES, phiRESET, and phiREAD are pulse signals supplied to a selection pixel line from said pulse selector 24 and phiRESET of them and phiREAD are activated within a horizontal blanking interval in the case of signal are recording actuation and signal read-out actuation, respectively, phiADRES is not generated in the case of signal are recording actuation, but is activated within a horizontal blanking interval in the case of signal read-out actuation.

[0129] In this case, the above-mentioned pulse signal phiADRES is generated so that the

selection control of the perpendicular selection line 6 of the same line may be carried out twice within the horizontal blanking interval in the case of signal read-out actuation and it may be in an active state twice intermittently for a reason which is mentioned later.

[0130] Next, actuation of the solid state camera of drawing 4 is explained, referring to drawing 6 and drawing 7 .

[0131] Since actuation of the solid state camera of drawing 4 is fundamentally the same compared with actuation (drawing 13) of the solid state camera (drawing 12) of the conventional example 1 mentioned above, explanation of the same actuation is omitted, and mainly different actuation is explained hereafter.

[0132] That is, in case the solid state camera of drawing 4 performs electronic shutter actuation, it is distributed to two perpendicular shift registers 21 and 22 only for [electronic shutter actuation / unit / field / alternation] electronic shutters by making the shift action of two perpendicular shift registers 21 and 22 for electronic shutters start by turns per field by the register change-over control circuit 23, and choosing each output by turns per field.

[0133] As shown at the field periods tFa and tFb in drawing 6 , even if timing signal phiES for signal storage-time control is inputted with a time interval shorter than a field period by this, it enables the perpendicular shift registers 21 and 22 only for electronic shutters to operate to coincidence.

[0134] In this case, it becomes possible to make sequential selection to the last of the pixel line for read-out, and to control the signal storage time of a selection pixel, without being reset on the way, before the perpendicular shift register 21 only for electronic shutters or the shift action of 22 reads and while having already started the shift action by timing signal phiESR1 or phiESR2 generated first finishes no selection control of the pixel lines of business.

[0135] If it puts in another way, it will become possible to realize electronic shutter ability (continuation electronic shutter actuation) to which the signal storage time is continuously changed per field, while the scan time of read-out has been fixed. In addition, in the same field, every selection pixel line of the signal storage time is the same.

[0136] Moreover, as shown in drawing 7 , pulse signal phiRESET and phiREAD are supplied to the pixel line of the n-th line which carried out the selection control to said level period tHES with the output signal ESn of shift [the n-th step of] stage of the perpendicular shift register for electronic shutters, and the signal charge of a photodiode is made into zero by reading the signal charge which was being accumulated before it with the photodiode PD of this pixel line of the n-th line to the gate of the transistor for magnification.

[0137] In this case, pulse signal phiADRES continues being "L", and since the transistor for perpendicular selection is still OFF, the signal charge read to the gate of said transistor for magnification is not outputted to the perpendicular signal line VLIN.

[0138] Then, in the case of the signal read-out actuation from said pixel line, after phiRESET is activated temporarily at the horizontal blanking interval in said level period tHRO, phiADRES is activated and phiREAD is activated further temporarily.

[0139] In this case, when the aforementioned phiREAD is an active state ("H" level), so that the diving of the noise under the effect of capacity coupling between a photodiode and its circumference wiring (phiADRES wiring later mentioned in this example) may

not occur phiADRES pulse is temporarily made into a non-active state ("L" level) so that it may be in the same condition as the time of signal are recording actuation, and this phiADRES is activating the aforementioned phiREAD temporarily within the period of a non-active state.

[0140] First, if the actuation at the time of signal read-out within the horizontal blanking interval in said such level period tHRO is explained in detail, after resetting the gate electrode of the magnification transistor Tb to a reference potential by phiRESET, phiADRES will be made into an active state (the 1st time), the perpendicular selection transistor Ta of said pixel line of the n-th line will be made into an ON state, pulse signal phiCLP supplied to a noise canceller circuit within this activity period will be activated, and black level will be clamped.

[0141] And when phiADRES activates phiREAD within the period of a non-active state, the signal charge which was being accumulated before it with said photodiode PD is read to the gate of the magnification transistor Tb.

[0142] And phiADRES is again made into an active state (the 2nd time), the perpendicular selection transistor Ta of said pixel line of the n-th line is again made into an ON state, and the signal charge read to the gate of said magnification transistor Tb is outputted to the perpendicular signal line VLIN.

[0143] By the above actuation, from the termination point in time of the active state ("H" level) of read line driving signal phiREAD in said level period tHES to the activation time of read line driving signal phiREAD in said level period tHRO serves as the signal storage time.

[0144] Drawing 8 (a) is the top view taking out and showing a part of unit cell of an image pick-up field, in order to explain the diving of said noise.

[0145] Drawing 8 (b) is a sectional view which meets the a-a'line of this drawing (a).

[0146] Drawing 8 (c) and (d) correspond, respectively, and when phiADRES in this drawing (a) is "L" level and it is /"H" level, they show the potential potential in the substrate in the case of phiREAD being activated and reading a signal charge. Here, the case where power-source potential is 3.3V is shown.

[0147] the P type with which 81 was formed in the surface section of a silicon substrate in drawing 8 (a) and (b) -- a well -- a field and 82 are the component isolation regions (for example, LOCOS field) alternatively formed in the substrate surface section. n mold field (detection node DN) used as n mold field which serves as the cathode field of a photodiode and the source field of the read-out transistor Td, and the drain field of the read-out transistor Td is alternatively formed in the component field of the substrate surface section.

[0148] On the channel field of the above-mentioned read-out transistor Td, the gate electrode (a part of read line 4) which consists of polish recon wiring through the insulated-gate film is formed, and the perpendicular selection line 5 and the reset line 7 which consist of polish recon wiring on the component isolation region 82 near the n mold field of Photodiode PD are formed in abbreviation parallel.

[0149] Since phiREAD is activated and a signal charge is read on the occasion of read-out actuation of the gestalt of this operation when phiADRES wiring contiguous to Photodiode PD is "L" level, as shown in drawing 8 (c), the potential potential in the substrate under Photodiode PD with the joint capacity calcium which exists between Photodiode PD and phiADRES wiring - Only VCa is reduced and the stored charge QCa

of Photodiode PD is read.
[0150] On the other hand, if phiREAD is activated and a signal charge is read when phiADRES wiring contiguous to Photodiode PD is "H" level, as shown in drawing 8 (d) By that from which the potential potential in the substrate under Photodiode PD can pull up only + VCa with the joint capacity calcium which exists between Photodiode PD and phiADRES wiring (it becomes the diving of a noise) When a part for the stored charge QCa of Photodiode PD is no longer read and the output signal of a solid state camera is displayed on the screen of an image display device, a black signal is crushed and it becomes an unsightly image.
[0151] Also in the solid state camera of the gestalt of implementation of the above 3rd in addition, like the solid state camera of the gestalt of said 2nd operation Add the 3rd dummy pixel line and the shift number of stages of the (2) 3 piece perpendicular selection circuitries 2, 21, and 22 is made into the number of stages of the pixel line count +1 for an original image pick-up. (1) -- said image pick-up field -- the 1- (3) When the driving signal for driving alternatively two or more horizontal control-line groups (4, 6, 7) based on the output of the perpendicular selection circuitries 2, 21, and 22 is generated by the pulse selector 24, The activation period of the last stage output signal of the perpendicular selection circuitry 2 chooses and drives the 1st dummy pixel line. The activation period of the last stage output signal of the 2nd perpendicular selection circuitry 21 chooses and drives the 2nd dummy pixel line, and the activation period of the last stage output signal of the 3rd perpendicular selection circuitry 22 may be constituted so that the 3rd dummy pixel line may be chosen and driven.
[0152] Such a configuration enables it for the pulse selector 24 to always come to carry out the selection drive of the pixel line per (a total of 3) respectively corresponding to each output of the perpendicular shift register 2 for read-out, and two perpendicular shift registers 21 and 22 for electronic shutters, and to prevent generating of the disk on the display screen resulting from fluctuation of the read-out level by the size of a selection load, since the selection load is always equal.
[0153] In addition, although the gestalt of said 3rd operation explained the case where phiADRES wiring existed as circumference wiring which the problem of black crushing by capacity coupling with Photodiode PD produces Since there is a possibility that the problem of crushing (black crushing) of the black signal by capacity coupling of these wiring and Photodiodes PD may arise also when phiRESET wiring or other wiring exist as the above-mentioned circumference wiring What is necessary is just to control level like phiADRES wiring in the gestalt of said 3rd operation also about these wiring.
[0154] namely, as applied voltage of circumference wiring of photodiodes PD other than read-out gate wiring which adjoins Photodiode PD as described above By impressing the same electrical potential difference as the activation period of signal read-out pulse phiREAD at the time of signal read-out actuation, and the activation period of read-out pulse phiREAD at the time of electronic shutter actuation it can come out and perform controlling so that an excessive charge is not read from Photodiode PD by capacity coupling of Photodiode PD and circumference wiring, and a reconstruction image without the so-called black crushing is acquired.
[0155] In addition, this invention is applicable also to the solid state camera which has the array of the unit cell of 2 pixels / 1 unit which is stated to the gestalt of the following operation [4th] according to the gestalt of said the operation of each.

[0156] <Gestalt of the 4th operation> drawing 9 shows the equal circuit of the unit cell of 2 pixels / 1 unit in the magnification mold CMOS solid state camera of the gestalt of the 4th operation. Since this CMOS solid state camera can be constituted like the gestalt of each operation mentioned above except the configuration of a unit cell, it mainly explains the configuration of the unit cell of 2 pixels / 1 unit hereafter.

[0157] The unit cell 30 shown in drawing 9 has two photodiodes 31a and 31b, touch-down potential is given to each anode side, each cathode side corresponds, respectively, and reads these two photodiodes 31a and 31b, and is connected common to the gate of one magnification transistor 33 through Transistors (shutter gate transistor) 32a and 32b. The read lines 4a and 4b are connected to each gate of the two above-mentioned read-out transistors 32a and 32b, respectively.

[0158] An end side is connected to the perpendicular signal line VLIN, the other end side is connected to the power-source line 9 through the perpendicular selection transistor 34 (that is, said magnification transistor 33 source follower connection), and, as for said magnification transistor 33, the perpendicular selection line (address line) 6 is connected to the gate of the above-mentioned perpendicular selection transistor 34.

[0159] Furthermore, one reset transistor 35 is connected between the gate of said magnification transistor 33, and the power-source line 9, and the reset line 7 is connected to the gate of this reset transistor 35.

[0160] The unit cell of 2 pixels / 1 unit of the above-mentioned configuration is arranged in the shape of [2-dimensional] a matrix to an image pick-up field. And said two read lines (1st read line 4a and 2nd read line 4b), perpendicular selection lines (address line) 6, and reset lines 7 are formed horizontally on an image pick-up field, and said perpendicular signal line VLIN and the power-source line 9 are perpendicularly formed on the image pick-up field.

[0161] Drawing 10 (a) shows an example of the flat-surface pattern of the unit cell of 2 pixels / 1 unit of drawing 9 , and shows drawing 10 (b) for the cross-section structure of meeting the B-B line, roughly.

[0162] In drawing 10 (a) and (b), 90 is an N type silicon substrate and P wells 91 are formed in the surface section. In the surface section of these P wells 91 The N type impurity range 931, the cathode field of photodiode 31b of another side used as the component isolation region (for example, LOCOS field) 92, the cathode field of one photodiode 31a, and the source field of one read-out transistor 32a And the N type impurity range 932 used as the source field of read-out transistor 32b of another side and the SDG field (only the N type impurity range 94 which reads to drawing and serves as a common drain of Transistors 32a and 32b is shown) of an NMOS transistor are formed alternatively.

[0163] And silicon oxide (gate dielectric film) 95 is formed on a substrate front face, and the field ion in plastic field 96 is formed in the bottom of the base of said LOCOS field 92.

[0164] Polish recon gate wiring whose 97 contains the gate electrode of the magnification transistor 33 in a part, the N type impurity range where 98 becomes the drain field of the magnification transistor 33 and the source field of the perpendicular selection transistor 34, and 99 are the N type impurity ranges used as the source field of the reset transistor 35.

[0165] 100 is wiring which connects the source field 99 of the reset transistor 35, the gate

wiring 97 of the magnification transistor 33, and the common drain field of two read-out transistors 32a and 32b.

[0166] Polish recon gate wiring whose read line 4a contains the gate electrode of read-out transistor 32a in a part, and read line 4b consist of polish recon gate wiring which contains the gate electrode of read-out transistor 32b in a part.

[0167] Polish recon gate wiring with which the perpendicular selection line (address line) 6 contains the gate electrode of the perpendicular selection transistor 34 in a part, and the reset line 7 consist of polish recon gate wiring which contains the gate electrode of the reset transistor 35 in a part.

[0168] 33a is the contact section of the source field of said magnification transistor 33, and the perpendicular signal line VLIN, and 34a is the contact section of the drain field of the above-mentioned perpendicular selection transistor 34, and the power-source line 9. For 97a, the contact section of the gate wiring 97 of the magnification transistor 33 and wiring 100 and 99a are [the contact section of the drain field of the reset transistor 35 and the power-source line 9 and 100a of the contact section of the source field 99 of the reset transistor 35 and wiring 100 and 99b] the contact sections of the above-mentioned wiring 100 and the common drain field of two read-out transistors 32a and 32b.

[0169] Although the basic actuation which actuation of the unit cell of 2 pixels / 1 unit of the above-mentioned configuration operates five transistors in predetermined sequence compared with actuation of the unit cell of said 1 pixel / 1 unit, and reads a signal charge from a photodiode is the same, the points which read a signal charge to timing which is different from two photodiodes 31a and 31b differ. That is, it is supposed that the read signal of "H" level is given to 1st read line 4a when reading a signal charge from one photodiode 31a, and the read signal of "L" level has been given to 2nd read line 4b. Suppose that the read signal of "H" level is given to 2nd read line 4b when reading a signal charge from photodiode 31b of another side, and the read signal of "L" level has been given to 1st read line 4a.

[0170] In the CMOS solid state camera which has <the gestalt of the 5th operation>, and the array of a unit cell of 2 pixels / 1 unit which was described above in time By driving an address-line driving signal twice intermittently, as it described above, when not giving electronic shutter ability which was described above and reading a signal charge to timing which is different from two photodiodes 31a and 31b It becomes possible to prevent the problem of generating of the disk on the display screen at the time of displaying an output signal on the screen of an image display device.

[0171] Drawing 11 is the timing wave form chart showing an example of signal read-out actuation of a part of 1 field period in the CMOS solid state camera of the gestalt of the 5th operation.

[0172] In drawing 11 , although phiRESET, phiADRES, phiREAD1, or phiREAD2 is a pulse signal supplied to a selection pixel line from a pulse selector and it activates within a horizontal blanking interval in the case of signal read-out actuation, respectively, phiREAD1 and phiREAD2 are supplied within a different horizontal blanking interval.

[0173] Here rather than the distance of the 1st read line 4a and the address line 6 to which phiREAD1 is supplied Since the distance of the 2nd read line 4b and the address line 6 to which phiREAD2 is supplied is short and the joint capacity of 2nd read line 4b and the address line 6 is larger than the joint capacity of 1st read line 4a and the address line 6 It originates in the effects to the signal charge read from two photodiodes 31a and 31b,

respectively differing, and there is a possibility that the disk on the display screen at the time of displaying an output signal on the screen of an image display device may occur.
[0174] However, phiADRES so that the selection control of the address line 6 of the same line may be carried out twice within the horizontal blanking interval in the case of signal read-out actuation Since phiADRES has "L" level, respectively when it is generated so that it may be in an active state twice intermittently, and reading a signal charge from two photodiodes 31a and 31b, respectively The problem of generating of the disk on the display screen which the effect of [at the time of the above-mentioned signal-charge read-out] becomes almost equal, and was described above can be prevented.
[0175] Moreover, this invention is applicable not only to the solid state camera of the type of the gestalt of each above-mentioned implementation but the solid state camera of the laminating mold which carried out the laminating of the photo-electric-conversion section.
[0176]
[Effect of the Invention] According to the solid state camera of each claim subordinate to claim 1 and it, when making electronic shutter actuation perform, fluctuation of the load of the perpendicular shift register for read-out and the perpendicular shift register for electronic shutters can be prevented, the image noise of the lateral stripe generated in the display screen of an output signal can be controlled, and the clear high image of S/N can be obtained.
[0177] According to the solid state camera of each claim subordinate to claim 3 and it, the good transformation child shutter actuation (continuation electronic shutter actuation) to which the signal storage time is changed per field is realizable by distributing electronic shutter actuation to the shift register only for [of two pieces] electronic shutters by turns per field. In this case, it can prevent that the difference of the signal storage time arises to pixel spacing according to the merits and demerits of the signal storage time, and generating of image noises, such as a lateral stripe in the display screen of an output signal, can be prevented.
[0178] according to especially the solid state camera of claim 4, continuation electronic shutter actuation is realizable like the solid state camera of claim 3 -- both Two dummy pixel lines are prepared corresponding to the perpendicular shift register only for [of two pieces] electronic shutters. By always carrying out the selection drive of the three pixel lines by which a selection control is carried out with the shift register for read-out, and the shift register only for [of two pieces] electronic shutters, fluctuation of the load accompanying pixel line selection is lost, and generating of the lateral stripe on the display screen can be prevented.
[0179] According to the solid state camera of each claim subordinate to claim 10 and it Electronic shutter actuation is realizable, and also the applied voltage of circumference wiring of those other than the read-out gate contiguous to a photodiode It considers as the same electrical potential difference in both the activation period of the read-out pulse signal at the time of signal read-out actuation, and the activation period of the read-out pulse signal at the time of electronic shutter actuation. A reconstruction image without black crushing is acquired by controlling read-out of the excessive charge from the photodiode by capacity coupling with wiring.
[0180] When reading stored charge from the 2-pixel optoelectric transducer in the unit cell of 2 pixels / 1 unit of an image pick-up field, respectively according to the solid state

camera of the claim subordinate to claim 12 and it, Since the electrical potential difference of other wiring which adjoins wiring which controls this read-out and exists around said optoelectric transducer is substantially made the same at the time of read-out of each pixel When reading a signal charge from a 2-pixel optoelectric transducer, respectively, the effect which the electrical potential difference of other wiring does becomes almost equal, and can prevent the problem of generating of the disk on the display screen.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] Drawing showing the equal circuit of the CMOS solid state camera of the gestalt of operation of the 1st of this invention.

[Drawing 2] Drawing showing the equal circuit of the CMOS solid state camera of the gestalt of operation of the 2nd of this invention.

[Drawing 3] The timing chart showing signs that two perpendicular shift registers for electronic shutters control electronic shutter actuation by turns per field in the solid state camera of drawing 2 .

[Drawing 4] Drawing showing the equal circuit of the CMOS solid state camera of the gestalt of operation of the 3rd of this invention.

[Drawing 5] The circuit diagram showing an example of the pulse selector in drawing 4 .

[Drawing 6] the timing generating circuit in drawing 4 , and perpendicular shift register [of ** a 1st] - the timing wave form chart showing the 3rd perpendicular shift register and the example of a pulse selector of operation.

[Drawing 7] It is the timing wave form chart showing an example of the electronic shutter actuation within 1 field period in drawing 6 .

[Drawing 8] Drawing showing the potential potential in the top view showing a part of unit cell of an image pick-up field in order to explain the actuation which controls the diving of a noise in the electronic shutter actuation shown in drawing 7 , a sectional view, and a substrate.

[Drawing 9] Drawing showing the equal circuit of the unit cell of 2 pixels / 1 unit in the magnification mold CMOS solid state camera of the gestalt of operation of the 4th of this invention.

[Drawing 10] Drawing showing roughly an example of the flat-surface pattern of the unit cell of 2 pixels / 1 unit of drawing 9 , and an example of the cross-section structure.

[Drawing 11] The timing wave form chart showing an example of the signal read-out actuation within 1 field period in the CMOS solid state camera of the gestalt of operation of the 5th of this invention.

[Drawing 12] Drawing showing the equal circuit of the CMOS solid state camera of the conventional example 1.

[Drawing 13] The timing wave form chart showing the example of the CMOS solid state camera of drawing 12 of operation.

[Drawing 14] The timing wave form chart showing the example of the timing generating circuit in drawing 13 , a perpendicular shift register, and a pulse selector of operation.

[Drawing 15] Drawing showing the equal circuit of the CMOS solid state camera of the conventional example 2.

[Drawing 16] Drawing showing an example of the line selection timing of two perpendicular shift registers in drawing 15 .
[Drawing 17] in order to change the signal storage time in the solid state camera of drawing 15 -- the perpendicular shift register for electronic shutters -- reading -- business -- the timing chart shown in order to explain the trouble in the case of changing the merits and demerits of the time amount which the timing which performs line selection ahead of a perpendicular shift register is changed, and accumulates a pixel signal.
[Description of Notations]
2 -- Perpendicular shift register for read-out,
3 -- Level shift register,
4 -- Read line,
6 -- Perpendicular selection line,
7 -- Reset line,
9 -- Power-source line,
10a -- Timing generating circuit,
21 22 -- Perpendicular shift register for electronic shutters,
23 -- Change-over control circuit,
24 -- Vertical-drive circuit (pulse selector),
PD -- Photodiode,
Ta -- Perpendicular selection transistor (line selection transistor),
Tb -- Magnification transistor,
Tc -- Reset transistor,
Td -- Read-out transistor,
TH -- Level selection transistor,
VLIN -- Perpendicular signal line,
HLIN -- Level signal line.

PRIOR ART

[Description of the Prior Art] Drawing 12 shows the equal circuit of the CMOS solid state camera (magnification mold CMOS image sensors) of the conventional example 1 equipped with the readout circuitry which a pixel signal can read for every pixel.
[0003] In drawing 12 , the unit cell of 1 pixel (1 pixel) / 1 unit is arranged in the shape of [which is two dimensions] a matrix, and is formed in the cel field (image pick-up field).
[0004] Each unit cell consists of four transistors Ta, Tb, Tc, and Td and one photodiode PD.
[0005] Namely, the photodiode PD with which touch-down potential is given to an anode side The read-out transistor Td by which the end side is connected to the cathode side of Photodiode PD (shutter gate transistor), The magnification transistor Tb by which the gate is connected to the other end side of the read-out transistor Td The reset transistor Tc by which the end side is connected to the gate of the perpendicular selection transistor (line selection transistor) Ta and the magnification transistor Tb where the end side is connected to the end side of the magnification transistor Tb is provided.
[0006] And corresponding to each pixel line, the perpendicular selection [which was connected common to the gate of each read-out transistor Td of the unit cell of the same line] line 6 connected with the line 4 common to the gate of each perpendicular selection

transistor Ta of the unit cell of the same line and the reset line 7 connected common to the gate of each reset transistor Tc of the unit cell of the same line are formed in said cel field by reading.

[0007] Moreover, corresponding to each pixel train, the power-source line 9 connected common to the other end [of each reset transistor Tc of the unit cell of the same train as the perpendicular signal line VLIN connected common to the other end side of each magnification transistor Tb of the unit cell of the same train] and other end side of each perpendicular selection transistor Ta is formed in said cel field.

[0008] Furthermore, in the exterior by the side of the end of a cel field, two or more load transistors TL connected, respectively between one one end each of said perpendicular signal line VLIN and a touch-down node are arranged horizontally.

[0009] Moreover, in the exterior by the side of the other end of a cel field, two or more noise canceller circuits which consisted of two transistors TSH and TCLP and two capacitors Cc and Ct are arranged horizontally.

[0010] And two or more level selection transistors TH connected to each other end side of said perpendicular signal line VLIN through each above-mentioned noise canceller circuit are arranged horizontally.

[0011] The level signal line HLIN is connected to each other end of the above-mentioned level selection transistor TH in common, and they are a level reset transistor (not shown) and the output amplifying circuit AMP in this level signal line HLIN. It connects.

[0012] In addition, the transistor TSH for sample hold by which, as for said each noise canceller circuit, the end side was connected to the other end side of the perpendicular signal line VLIN Coupling-capacitor Cc by which the end side was connected to the other end side of the transistor TSH for these sample hold, The capacitor Ct for charge storages connected between touch-down nodes the other end side of this coupling-capacitor Cc, It is constituted by the transistor TCLP for a potential clamp connected to the connection node of said capacitors Cc and Ct, and the end side of said level selection transistor TH is connected to the connection node of said capacitors Cc and Ct.

[0013] furthermore, in the exterior of a cel field Two or more perpendicular selection lines 6 of a cel field The timing generating circuit 10 which generates various kinds of timing signals for supplying the perpendicular shift register 2 for carrying out a selection control in scan, and said level selection transistor TH to the level shift register 3 for driving in scan, said noise canceller circuit, etc., The bias generating circuit 11 for generating predetermined bias potential at the end of the transistor TCLP for the potential clamp of said noise canceller circuit etc., Pulse selector 2a for carrying out the selection control of the output pulse of the above-mentioned perpendicular shift register 2, and driving the perpendicular selection line 6 of each line of a cel field in scan is arranged, respectively.

[0014] Drawing 13 is the timing wave form chart showing an example of actuation of the solid-state image sensors shown in drawing 12 .

[0015] Next, actuation of the solid-state image sensors of drawing 12 is explained, referring to drawing 13 .

[0016] The signal charge which photo electric conversion of the incident light of each photodiode PD was carried out, and it produced is accumulated into Photodiode PD.

[0017] In a horizontal blanking interval, in case the signal charge of Photodiode PD is read from the unit cell for a certain party, in order to choose each perpendicular signal

line VLIN, the line selection transistor Ta for a party is first turned ON by turning ON the signal (phiADRES pulse) of the perpendicular selection line 6 of the line for selection.

[0018] The source follower circuit which consists of a magnification transistor Tb to which the power-source potential VDD (for example, 3.3V) is supplied through the line selection transistor Ta, and a load transistor TL in the unit cell for said party by this is operated.

[0019] Next, in the unit cell for said party, reference voltage is outputted to the perpendicular signal line VLIN by turning ON the signal (phiRESET pulse) of the reset line 7, and carrying out fixed period reset of the gate voltage of the magnification transistor Tb at reference voltage.

[0020] However, as described above, dispersion exists in the gate potential of the reset magnification transistor Tb, and dispersion appears also in the reset potential of the perpendicular signal line VLIN by the side of the other end.

[0021] Then, in order to reset dispersion in the reset potential of each perpendicular signal line VLIN The driving signal (phiSH pulse) of the transistor TSH for sample hold in a noise canceller circuit is turned ON beforehand (for example, the aforementioned phiADRES to ON and coincidence of a pulse). After reference voltage is outputted to said perpendicular signal line VLIN, by making the driving signal (phiCLP pulse) of the transistor TCLP for a potential clamp fixed time amount ON, reference voltage is set as the connection node of the capacitors Cc and Ct of a noise canceller circuit.

[0022] Next, aforementioned phiRESET After turning off a pulse, by choosing the read line 4 of a predetermined line and turning on the signal (phiREAD pulse), the read-out transistor Td is turned ON and gate potential is changed by reading the stored charge of Photodiode PD to the gate of the magnification transistor Tb. The magnification transistor Tb outputs the voltage signal according to the variation of gate potential to the corresponding perpendicular signal line VLIN and a noise canceller circuit.

[0023] Then, a level effective scan term period can also accumulate the signal component (signal level from which the noise was removed) equivalent to the difference of the reference voltage read as described above, and a signal level in the capacitor Ct for charge storages by turning off phiSH pulse in a noise canceller circuit.

[0024] That is, the noise mixed in the preceding paragraph side from noise canceller circuits, such as dispersion in the reset potential of each perpendicular signal line VLIN resulting from a cel field, is removed.

[0025] And phiADRES By the perpendicular selection transistor's Ta being controlled by the OFF state, and changing a unit cell into the condition of not choosing, a cel field and each noise canceller circuit are electrically separated by turning OFF a pulse.

[0026] By making sequential ON the driving signal (phiH pulse) of the level selection transistor TH at a next horizontal effective scan period, the level selection transistor TH is turned on [sequential], the signal level of the connection node (signal preservation node) of said capacitors Cc and Ct is read to the level signal line HLIN one by one, and it is the output amplifying circuit AMP. It is amplified and outputs.

[0027] It sets in the above-mentioned actuation and is the electrical potential difference VVLIN of the perpendicular signal line VLIN. Noise rejection actuation which becomes the operating voltage Vm (about 1.5 V) of a source follower circuit and which was described in addition above is performed for every read-out actuation for every horizontal line at a horizontal blanking interval.

[0028] Drawing 14 is the timing wave form chart showing the timing generating circuit 10 in drawing 13 , the perpendicular shift register 2, and the example of pulse selector 2a of operation.
[0029] Here, the case where the solid state camera of drawing 12 is used by 1 field =1 / 30Hz (image of 30 frames per second which make the 1 field one frame) system is shown.
[0030] The timing generating circuit 10 operates external input pulse signal phiVR and phiHP orthopedically in a buffer circuit, and is pulse signal phiVRR of a field period. Pulse signal phiHPV of a level period It inputs into said perpendicular shift register 2.
[0031] The perpendicular shift register 2 is pulse signal phiVRR. Pulse signal phiHPV after an input clears all register outputs at the period of "L" level and makes it "L" level A shift action is performed, and the output pulse signal ROi (i=--, n, n+1, --) is made into "H" level one by one, and is inputted into said pulse selector 2a.
[0032] Pulse selector 2a activates the signal (phiADRES pulse) of the perpendicular selection line 6, the signal (phiRESET pulse) of the reset line 7, and the signal (phiREAD pulse) of the read line 4, as shown in drawing 13 to each line for selection, and it scans the line for selection.
[0033] It is each output pulse signal ROi of the perpendicular shift register 2 for the solid state camera of drawing 12 to carry out the selection control of the specific line for selection, as described above. It outputs only once within 1 field period. That is, since Photodiode PD performs signal read-out in the 1 field only once, the electronic shutter actuation which controls light-receiving time amount equivalent is impossible by controlling the signal storage time of Photodiode PD.
[0034] On the other hand, drawing 15 shows roughly the configuration of the CMOS solid state camera of the conventional example 2 in which electronic shutter actuation is possible.
[0035] This solid state camera For example, the image pick-up field 14 where the pixel cel 13 constituted as shown in drawing 12 has been arranged two-dimensional in the shape of a matrix (photo-electric-conversion section), Two or more perpendicular signal lines VLIN formed in the direction of a pixel train of said image pick-up field 14 Two or more perpendicular selection lines 6 for read-out control for controlling to be formed in the pixel line writing direction of said image pick-up field 14, and to read the photo-electric-conversion signal of each pixel cel 13 to said two or more perpendicular signal lines VLIN per pixel line, The 1st perpendicular selection circuitry 2 for carrying out a selection control in scan to the timing of read-out of said two or more perpendicular selection lines 6 for read-out control (perpendicular shift register for read-out), The level selection transistor TH for choosing said perpendicular signal line VLIN, The level selection circuitry 3 for carrying out the selection control of said level selection transistor (level selection shift register), Output amplifying circuit AMP for outputting the signal read to the level signal line HLIN and said level signal line HLIN for reading the signal of said perpendicular signal line VLIN chosen with said level selection shift register 3 It provides.
[0036] In addition, especially the point equipped with a load transistor as shown in drawing 12 , a noise canceller circuit, etc. around the image pick-up field 14 although not illustrated is the same as that of the CMOS solid state camera of an example 1.
[0037] Furthermore, the vertical-drive circuit (not shown) which generates the driving

signal for driving alternatively said two or more perpendicular selection lines 6 for read-out control based on the output of the 2nd perpendicular selection circuitry (perpendicular shift register for electronic shutters) 15 for carrying out a selection control in scan and said 1st perpendicular selection circuitry and the output of the 2nd perpendicular selection circuitry to the timing of signal are recording of said two or more perpendicular selection lines 6 for read-out control is provided.

[0038] That is, the perpendicular shift register 15 for electronic shutters is formed independently [the perpendicular shift register 2 for read-out], and it is constituted so that this perpendicular shift register 15 for electronic shutters as well as the perpendicular shift register 2 for read-out may scan the line for selection to predetermined timing.

[0039] Thereby, the perpendicular shift register 2 for read-out and the perpendicular shift register 15 for electronic shutters enable it to carry out the selection control of the specific line for selection to 2 times of timing within 1 field period.

[0040] Therefore, when the perpendicular shift register 15 for electronic shutters carries out the selection control of the line for selection and starts are recording of a pixel signal before the twist from which the perpendicular shift register 2 for read-out carries out the selection control of the line for selection, and reads a pixel signal to the perpendicular signal line VLIN, the electronic shutter actuation which controls light-receiving time amount equivalent is attained.

[0041] By the way, the CMOS solid state camera of drawing 15 which has one perpendicular shift register 2 for read-out and one perpendicular shift register 15 for electronic shutters which were described above For example, when making the good transformation child shutter actuation to which light-receiving time amount is changed equivalent by changing the signal storage time automatically according to the output level of a photo sensor perform There is a problem of the difference of the signal storage time arising to pixel spacing, or changing the load of two perpendicular shift registers 2 and 15 to it according to the merits and demerits of the signal storage time.

[0042] This problem is explained below.

[0043] Drawing 16 shows an example in case the line selection timing of two perpendicular shift registers 2 and 15 in drawing 15 is immobilization.

[0044] As shown in drawing 16 , the timing to which the perpendicular shift register 15 for electronic shutters performs line selection ahead of the perpendicular shift register 2 for read-out is being fixed, that is, the two above-mentioned perpendicular shift registers 2 and 15 of the time difference which performs line selection are always fixed.

[0045] Thus, when the line selection timing of two perpendicular shift registers 2 and 15 is immobilization, the perpendicular shift register 2 for read-out and the perpendicular shift register 15 for electronic shutters begin selection of return and the following frame to the first rank again, after it begins selection of a certain frame and the shift action from the first rank to a tail end (that is, the number of pixels of the perpendicular direction of a solid state camera) finishes.

[0046] Therefore, the solid state camera of drawing 15 has the problem of the difference of the signal storage time arising to pixel spacing, or changing the load of two perpendicular shift registers 2 and 15 to it according to the merits and demerits of the signal storage time, when making the good transformation child shutter actuation to which light-receiving time amount is changed equivalent by changing the signal storage time automatically according to the output level of a photo sensor perform.

[0047] Here, said problem is stated to a detail, referring to drawing 17 about the case where the merits and demerits of the time amount in which the perpendicular shift register 15 for electronic shutters changes the timing (timing of an electronic shutter) which performs line selection ahead of the perpendicular shift register 2 for read-out, and accumulates a pixel signal as concrete technique for changing the signal storage time are changed.

[0048] In drawing 17 , a read-out control pulse is a signal which makes the shift action of the perpendicular shift register 2 for read-out start, and a good transformation child shutter control pulse is a signal which makes the shift action of the perpendicular shift register 15 for electronic shutters start.

[0049] (1) After starting the shift action of the perpendicular shift register 15 for electronic shutters by the control pulse of the electronic shutter generated to the timing t1 in drawing 17 on the occasion of selection of the 1st frame, before the shift action to a tail end finishes (before choosing all pixel lines), in order to choose the 2nd frame to the timing t3 in drawing 17 , suppose that the electronic shutter pulse occurred. In this case, the perpendicular shift register 15 for electronic shutters is reset to the above-mentioned timing t3, and starts a shift action (line selection) from the first rank again.

[0050] Thereby, in case [at which it generated to the timing t2 in drawing 17] it reads, and the shift action of the perpendicular shift register 2 for read-out begins by the control pulse and said 1st frame is read, the difference of the signal storage time arises in the pixel line by which selection assignment was not carried out with the pixel line by which selection assignment was carried out with the perpendicular shift register 15 for electronic shutters which the shift action started to said timing t1.

[0051] Thus, if the difference of the signal storage time arises, when a read-out output level is changed depending on the location of a pixel line and displays the output signal of a solid state camera on the screen of an image display device, it will become the cause which image noises, such as a lateral stripe, generate.

[0052] (2) in the timing t4 in drawing 17 , the shift action began to the selection line and said timing t2 of the perpendicular shift register 15 for electronic shutters which the shift action started to said timing t3 -- reading -- business -- since a total of two pixel lines of the selection line of the perpendicular shift register 2 are chosen, these two pixel lines serve as a load of two perpendicular shift registers 2 and 15.

[0053] on the other hand, in the timing t6 in drawing 17 , the selection line by the perpendicular shift register 15 for electronic shutters which the shift action started to said timing t3 did not already exist, but the shift action started it to the timing t5 in drawing 17 -- reading -- business -- since one pixel line is chosen with the perpendicular shift register 2, this one pixel line serves as a load of two perpendicular shift registers 2 and 15.

[0054] Thus, if the load of two perpendicular shift registers 2 and 15 is changed depending on electronic shutter timing, the voltage variation of power-source Rhine of a solid state camera is imitated, and it comes, and when the output signal of a solid state camera is displayed on the screen of an image display device, a lateral stripe will be generated, and it will become the cause which worsens image quality notably.

[0055] In addition, the problem of the difference of the signal storage time arising to pixel spacing, or changing the load of two perpendicular shift registers 2 and 15 to it according to the merits and demerits of the signal storage time which was described

above is produced not only the solid state camera of a CMOS mold but when making the solid state camera of a CCD mold perform good transformation child shutter actuation.

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ABSTRACT:

PROBLEM TO BE SOLVED: To provide a solid-state image pickup device capable of preventing the fluctuation of the loads of a vertical shift register for read and the vertical shift register for an electronic shutter in the case of performing an electronic shutter operation and preventing the generation of image noise such as horizontal stripes on the display screen of output signals.

SOLUTION: This device is provided with an image pickup area where a unit cell provided with a photodiode PD to be a pixel is two-dimensionally arranged, plural read lines 4 for driving the read transistor Td of each pixel row, plural vertical selection lines 6 for driving the vertical selection transistor Ta of each of the pixel rows, a vertical driving circuit 24 for selectively driving the plural read lines 4 and selectively driving the plural vertical selection lines 6, plural vertical signal lines VLIN for outputting signals from each unit cell of the successively driven pixel rows and row selection circuits 2, 21 and 22 for controlling the vertical driving circuit so as to successively drive the read transistor Td of each pixel two times at a desired signal storage timing and a signal read timing and to drive the vertical selection transistor Ta of the pixel row at the signal read timing.

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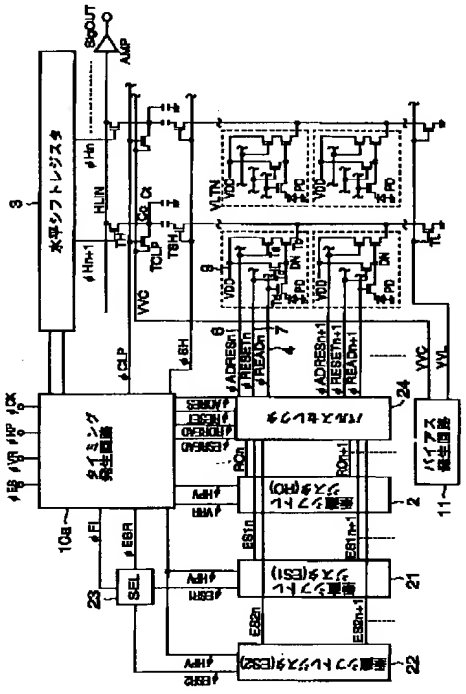
最終頁に続く

(54)【発明の名称】　固体撮像装置

(57)【要約】
【課題】固体撮像装置の可変（連続）電子シャッタ動作を実現する。
【解決手段】画素となるフォトダイオードPDを有する単位セルが二次元的に配置された撮像領域と、各画素行の読み出しトランジスタTdを駆動するための複数本の読取り線４と、各画素行の垂直選択トランジスタTaを駆動するための複数本の垂直選択線６と、複数本の読取り線を選択的に駆動し、複数本の垂直選択線を選択的に駆動する垂直駆動回路24と、順次駆動された画素行の各単位セルから信号が出力する複数の垂直信号線VLINと、各画素行の読み出しトランジスタを所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に２回駆動させ、信号読み出しタイミングで画素行の垂直選択トランジスタを駆動させるように垂直駆動回路を制御する行選択回路2,21,22 を具備する。



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【特許請求の範囲】

【請求項1】　画素に対する入射光を光電変換して電荷を蓄積する光電変換手段、蓄積した電荷を検出部に読み出す読み出し手段、読み出された電荷を増幅する増幅手段、前記検出部の電荷をリセットするためのリセット手段および前記増幅手段から信号を出力させる垂直選択手段を有する単位セルが半導体基板上に二次元的に配置されてなり、複数の信号読み出し用の画素行および少なくとも2つのダミー画素行を有する撮像領域と、

前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各読み出し手段を駆動するための読み出し駆動信号を伝送するための複数本の読取り線と、

前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各垂直選択手段を駆動するための行選択駆動信号を伝送するための複数本の垂直選択線と、

前記複数本の読取り線に読み出し駆動信号を選択的に供給して前記読み出し手段を駆動するとともに、前記複数本の垂直選択線に行選択駆動信号を選択的に供給して前記垂直選択手段を駆動するための垂直駆動手段と、

前記撮像領域における各画素行の読み出し手段を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に2回駆動させるように前記垂直駆動手段を制御する行選択手段と、

前記撮像領域における各画素列に対応して設けられ、前記垂直駆動手段により順次駆動された画素行の各単位セルからそれぞれ出力される信号を垂直方向に伝送するための複数の垂直信号線とを具備し、

前記行選択手段は、

前記垂直駆動手段により前記複数の信号読み出し用の画素行の単位セルからの信号読み出しを制御した後、前記2つのダミー画素行のうちの第1のダミー画素行を駆動させるように選択制御し、前記垂直駆動手段により前記複数の信号読み出し用の画素行の単位セルにおける信号蓄積を制御した後、前記前記2つのダミー画素行のうちの第2のダミー画素行を駆動させるように選択制御することを特徴とする固体撮像装置。

【請求項2】　請求項1記載の固体撮像装置において、

前記行選択手段は、

前記単位セルにおける信号蓄積の開始期間を制御するための電子シャッタ用のシフトレジスタと、

前記単位セルからの信号読み出しの開始期間を制御するための読み出し用のシフトレジスタを有し、

前記第1のダミー画素行は、前記読み出し用のシフトレジスタにより選択制御され、前記第2のダミー画素行は、前記電子シャッタ用のシフトレジスタにより選択制御されることを特徴とする固体撮像装置。

【請求項3】　画素に対する入射光を光電変換して電荷を蓄積する光電変換手段、蓄積した電荷を検出部に読み出す読み出し手段、読み出された電荷を増幅する増幅手段、前記検出部の電荷をリセットするためのリセット手段および前記増幅手段から信号を出力させる垂直選択手段を有する単位セルが半導体基板上に二次元的に配置されてなり、複数の画素行を有する撮像領域と、

前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各読み出し手段を駆動するための読み出し駆動信号を伝送するための複数本の読取り線と、

前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各垂直選択手段を駆動するための行選択駆動信号を伝送するための複数本の垂直選択線と、

前記複数本の読取り線に読み出し駆動信号を選択的に供給して前記読み出し手段を駆動するとともに、前記複数本の垂直選択線に行選択駆動信号を選択的に供給して前記垂直選択手段を駆動するための垂直駆動手段と、

前記撮像領域における各画素行の読み出し手段を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に2回駆動させるように前記垂直駆動手段を制御する行選択手段と、

前記撮像領域における各画素列に対応して設けられ、前記垂直駆動手段により順次駆動された画素行の各単位セルからそれぞれ出力される信号を垂直方向に伝送するための複数の垂直信号線とを具備し、

前記行選択手段は、

前記垂直駆動手段により前記信号読み出しタイミングで前記各画素行の読み出し手段を駆動させる第1の手段と、前記垂直駆動手段により前記信号蓄積タイミングで前記各画素行の読み出し手段を駆動させる少なくとも2個の第2の手段とを具備することを特徴とする固体撮像装置。

【請求項4】　請求項3記載の固体撮像装置において、

前記撮像領域は、信号読み出し用の前記複数の画素行のほかに少なくとも3本のダミー画素行をさらに具備し、

前記行選択手段は、前記第1の手段により前記ダミー画素行のうちの1つのダミー画素行を駆動させ、前記2個の第2の手段により前記ダミー画素行のうちの他の2つのダミー画素行を駆動させることを特徴とする固体撮像装置。

【請求項5】　請求項3または4記載の固体撮像装置において、

前記行選択手段は、各画素行の信号読み出しタイミングの周期に対応する1フィールド単位で1フィールド周期の期間内における信号蓄積タイミングを変化させることを特徴とする固体撮像装置。

【請求項6】　請求項5記載の固体撮像装置において、

前記少なくとも2個の第2の手段は、互いに前記信号読み出しタイミングに対する信号蓄積タイミングを相対的に異ならせて前記読み出し手段を駆動させるものであ

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り、前記第2の手段による前記垂直駆動手段の制御動作が1フィールド毎に交互に切換えられることを特徴とする固体撮像装置。

【請求項7】　請求項5記載の固体撮像装置において、前記行選択手段の第1の手段は、前記単位セルからの信号読み出しの開始期間を制御するための読み出し用のシフトレジスタを具備し、

前記行選択手段の第2の手段は、第1のフィールド期間での前記単位セルにおける信号蓄積の開始期間を制御するための第1の電子シャッタ用のシフトレジスタおよび前記第1のフィールド期間と交互に繰り返される第2のフィールド期間での前記単位セルにおける信号蓄積の開始期間を制御するための第2の電子シャッタ用のシフトレジスタを具備することを特徴とする固体撮像装置。

【請求項8】　請求項1乃至7のいずれか1つに記載の固体撮像装置において、

前記行選択手段は、前記撮像領域における各画素行の読み出し手段を2回駆動させる際、前記光電変換手段の周辺で前記読取り線に隣接する他の配線の電圧を前記2回の駆動時とも実質的に同一にするように前記垂直駆動手段を制御することを特徴とする固体撮像装置。

【請求項9】　請求項8記載の固体撮像装置において、前記読取り線に隣接する他の配線は、前記垂直選択線であることを特徴とする固体撮像装置。

【請求項10】　半導体基板上の撮像領域に二次元的に配置された単位セルの光電変換素子から蓄積電荷を読み出す際、この読み出しを制御する配線を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に2回駆動させ、前記信号読み出しタイミングで読み出された信号を出力させる電子シャッタ動作を行う固体撮像装置において、

前記読み出しを制御する配線に隣接し、前記光電変換素子の周辺に存在する他の配線の電圧を前記信号蓄積タイミングと信号読み出しタイミングとで実質的に同一にすることを特徴とする固体撮像装置。

【請求項11】　請求項1乃至10のいずれか1つに記載の固体撮像装置において、

前記単位セルは、

アノード側に接地電位が与えられる1個のフォトダイオードと、

前記1個のフォトダイオードのカソード側に一端側が接続され、ゲートに読取り線が接続された1個の読み出しトランジスタと、

前記読み出しトランジスタの他端側にゲートが接続され、一端側に垂直信号線が接続された1個の増幅トランジスタと、

前記増幅トランジスタの他端側に一端側が接続され、ゲートには垂直選択線が接続された1個の垂直選択トランジスタと、

前記垂直選択トランジスタの他端側に接続された1本の電源線と、

前記増幅トランジスタのゲートと前記電源線との間に接続され、ゲートにはリセット線が接続された1個のリセットトランジスタとを具備し、前記1個のフォトダイオードが1つの画素に対応することを特徴とする固体撮像装置。

【請求項12】　2画素／1ユニットの単位セルが半導体基板上に二次元的に配置されてなる撮像領域を有する固体撮像装置において、

前記撮像領域の単位セルにおける2画素の光電変換素子からそれぞれ蓄積電荷を読み出す際、この読み出しを制御する配線に隣接し、前記光電変換素子の周辺に存在する他の配線の電圧を各画素の読み出し時で実質的に同一にすることを特徴とする固体撮像装置。

【請求項13】　請求項1乃至12のいずれか1つに記載の固体撮像装置において、

前記単位セルは、

各アノード側に接地電位が与えられる2個のフォトダイオードと、

前記2個のフォトダイオードの各カソード側にそれぞれ対応して各一端側が接続され、各ゲートに2本の読取り線がそれぞれ対応して接続された2個の読み出しトランジスタと、

前記2個の読み出しトランジスタの各他端側に共通にゲートが接続され、一端側に垂直信号線が接続された1個の増幅トランジスタと、

前記増幅トランジスタの他端側に一端側が接続され、ゲートには前記垂直選択線が接続された1個の垂直選択トランジスタと、

前記垂直選択トランジスタの他端側に接続された1本の電源線と、

前記増幅トランジスタのゲートと前記電源線との間に接続され、ゲートにはリセット線が接続された1個のリセットトランジスタを具備し、

前記2個のフォトダイオードが2つの画素に対応することを特徴とする固体撮像装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、固体撮像装置に係り、特に固体撮像装置の可変電子シャッタ制御回路および画素信号読み出し制御回路に関するもので、例えばビデオカメラ、電子スティールカメラなどに使用される。

【0002】

【従来の技術】図12は、1画素毎に画素信号の読み出しが可能な読み出し回路を備えた従来例1のCMOS固体撮像装置（増幅型CMOSイメージセンサ）の等価回路を示している。

【0003】図12において、セル領域（撮像領域）には1ピクセル（1画素）／1ユニットの単位セルが二次元の行列状に配置されて形成されている。

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【0004】各単位セルは、例えば4個のトランジスタTa、Tb、Tc、Tdと、1個のフォトダイオードPDから構成される。

【0005】即ち、アノード側に接地電位が与えられるフォトダイオードPDと、フォトダイオードPDのカソード側に一端側が接続されている読み出しトランジスタ（シャッタゲートトランジスタ）Tdと、読み出しトランジスタTdの他端側にゲートが接続されている増幅トランジスタTbと、増幅トランジスタTbの一端側に一端側が接続されている垂直選択トランジスタ（行選択トランジスタ）Taと、増幅トランジスタTbのゲートに一端側が接続されているリセットトランジスタTcとを具備する。

【0006】そして、前記セル領域には、各画素行に対応して、同一行の単位セルの各読み出しトランジスタTdのゲートに共通に接続された読取り線4と、同一行の単位セルの各垂直選択トランジスタTaのゲートに共通に接続された垂直選択線6と、同一行の単位セルの各リセットトランジスタTcのゲートに共通に接続されたリセット線7が形成されている。

【0007】また、前記セル領域には、各画素列に対応して、同一列の単位セルの各増幅トランジスタTbの他端側に共通に接続された垂直信号線VLINと、同一列の単位セルの各リセットトランジスタTcの他端側および各垂直選択トランジスタTaの他端側に共通に接続された電源線9が形成されている。

【0008】さらに、セル領域の一端側の外部には、前記垂直信号線VLINの各一端側と接地ノードとの間にそれぞれ接続された複数の負荷トランジスタTLが水平方向に配置されている。

【0009】また、セル領域の他端側の外部には、例えば2個のトランジスタTSH、TCLPと2個のコンデンサCc、Ctから構成された複数のノイズキャンセラ回路が水平方向に配置されている。

【0010】そして、上記各ノイズキャンセラ回路を介して前記垂直信号線VLINの各他端側に接続された複数の水平選択トランジスタTHが水平方向に配置されている。

【0011】上記水平選択トランジスタTHの各他端に共通に水平信号線HLINが接続されており、この水平信号線HLINには水平リセットトランジスタ（図示せず）および出力増幅回路AMP が接続されている。

【0012】なお、前記各ノイズキャンセラ回路は、垂直信号線VLINの他端側に一端側が接続されたサンプルホールド用のトランジスタTSHと、このサンプルホールド用のトランジスタTSHの他端側に一端側が接続された結合コンデンサCcと、この結合コンデンサCcの他端側と接地ノードとの間に接続された電荷蓄積用のコンデンサCtと、前記コンデンサCc、Ctの接続ノードに接続された電位クランプ用のトランジスタTCLPとにより構

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成されており、前記コンデンサCc、Ctの接続ノードに前記水平選択トランジスタTHの一端側が接続されている。

【0013】さらに、セル領域の外部には、セル領域の複数の垂直選択線6を走査的に選択制御するための垂直シフトレジスタ2、前記水平選択トランジスタTHを走査的に駆動するための水平シフトレジスタ3、前記ノイズキャンセラ回路などに供給するための各種のタイミング信号を発生するタイミング発生回路10と、前記ノイズキャンセラ回路の電位クランプ用のトランジスタTCLPの一端などに所定のバイアス電位を発生するためのバイアス発生回路11と、上記垂直シフトレジスタ2の出力パルスを選択制御してセル領域の各行の垂直選択線6を走査的に駆動するためのパルスセレクタ2aとがそれぞれ配置されている。

【0014】図13は、図12に示した固体イメージセンサの動作の一例を示すタイミング波形図である。

【0015】次に、図13を参照しながら、図12の固体イメージセンサの動作を説明する。

【0016】各フォトダイオードPDの入射光が光電変換されて生じた信号電荷はフォトダイオードPD内に蓄積される。

【0017】水平帰線期間において、ある一行分の単位セルからフォトダイオードPDの信号電荷を読み出す際、まず、各垂直信号線VLINを選択するために、選択対象行の垂直選択線6の信号（φADRES パルス）をオンにすることにより一行分の行選択トランジスタTaをオンにする。

【0018】これにより、前記一行分の単位セルにおいて、行選択トランジスタTaを介して電源電位VDD（例えば3．3V）が供給される増幅トランジスタTbと負荷トランジスタTLからなるソースフォロワ回路を動作させる。

【0019】次に、前記一行分の単位セルにおいて、リセット線7の信号（φRESET パルス）をオンにし、増幅トランジスタTbのゲート電圧を基準電圧に一定期間リセットすることにより、垂直信号線VLINに基準電圧を出力する。

【0020】しかし、前記したようにリセットされた増幅トランジスタTbのゲート電位にはばらつきが存在し、その他端側の垂直信号線VLINのリセット電位にもばらつきが現われる。

【0021】そこで、各垂直信号線VLINのリセット電位のばらつきをリセットするために、予め（例えば前記φADRES パルスのオンと同時に）ノイズキャンセラ回路におけるサンプルホールド用トランジスタTSHの駆動信号（φSHパルス）をオンにしておき、前記垂直信号線VLINに基準電圧が出力された後に電位クランプ用のトランジスタTCLPの駆動信号（φCLP パルス）を一定時間オンにすることにより、ノイズキャンセラ回路のコンデンサC

ｃ、Ｃｔの接続ノードに基準電圧を設定する。

【００２２】次に、前記φRESET パルスをオフした後、所定行の読取り線４を選択してその信号（φREADパルス）をオンすることにより、読み出しトランジスタＴｄをオンにし、フォトダイオードＰＤの蓄積電荷を増幅トランジスタＴｂのゲートに読み出すことによりゲート電位を変化させる。増幅トランジスタＴｂは、ゲート電位の変化量に応じた電圧信号を対応する垂直信号線VLINおよびノイズキャンセラ回路に出力する。

【００２３】この後、ノイズキャンセラ回路におけるφSHパルスをオフすることにより、前記したように読み出された基準電圧と信号電圧の差分に相当する信号成分（ノイズが除去された信号電圧）を電荷蓄積用のコンデンサＣｔに水平有効走査期間中も蓄積することができる。

【００２４】つまり、セル領域に起因する各垂直信号線VLINのリセット電位のばらつきなどのノイズキャンセラ回路より前段側に混入したノイズは除去される。

【００２５】そして、φADRES パルスをオフにすることにより垂直選択トランジスタＴａがオフ状態に制御されて単位セルが非選択状態にされることにより、セル領域と各ノイズキャンセラ回路とが電気的に分離される。

【００２６】この後の水平有効走査期間に水平選択トランジスタＴＨの駆動信号（φH パルス）を順次オンにすることにより、水平選択トランジスタＴＨが順次オンになり、前記コンデンサＣｃ、Ｃｔの接続ノード（信号保存ノード）の信号電圧が水平信号線HLINに順次読み出され、出力増幅回路AMP により増幅されて出力する。

【００２７】上記動作において、垂直信号線VLINの電圧VVLIN は、水平帰線期間にはソースホロワ回路の動作電圧Ｖｍ（約１．５Ｖ）になる

なお、前記したノイズ除去動作は１水平線毎の読み出し動作毎に行われる。

【００２８】図１４は、図１３中のタイミング発生回路１０、垂直シフトレジスタ２およびパルスセレクタ２ａの動作例を示すタイミング波形図である。

【００２９】ここでは、図１２の固体撮像装置が１フィールド＝１／３０Ｈｚ（１フィールドを１フレームとする３０フレーム／秒の画像）のシステムで使用される場合を示している。

【００３０】タイミング発生回路１０は、外部入力パルス信号φVRとφHPをバッファ回路で整形し、フィールド周期のパルス信号φVRR と水平周期のパルス信号φHPV を前記垂直シフトレジスタ２へ入力する。

【００３１】垂直シフトレジスタ２は、パルス信号φVRR 入力が“Ｌ”レベルの期間にレジスタ出力を全てクリアして“Ｌ”レベルにした後、パルス信号φHPV によりシフト動作を行って出力パルス信号ROi （i=…,n,n+1,…）を順次“Ｈ”レベルにし、前記パルスセレクタ２ａに入力する。

【００３２】パルスセレクタ２ａは、各選択対象行に対して垂直選択線６の信号（φADRESパルス）、リセット線７の信号（φRESET パルス）、読取り線４の信号（φREADパルス）を図１３に示したように活性化し、選択対象行を走査する。

【００３３】上記したように、図１２の固体撮像装置は、特定の選択対象行を選択制御するための垂直シフトレジスタ２の各出力パルス信号ROi を、１フィールド期間内に１回しか出力しない。即ち、フォトダイオードＰＤは、１フィールドに１回しか信号読み出しを行わないので、フォトダイオードＰＤの信号蓄積時間を制御することによって等価的に受光時間を制御する電子シャッタ動作は不可能である。

【００３４】一方、図１５は、電子シャッタ動作が可能な従来例２のＣＭＯＳ固体撮像装置の構成を概略的に示している。

【００３５】この固体撮像装置は、例えば図１２に示したように構成される画素セル１３が行列状に二次元的に配置された撮像領域（光電変換部）１４と、前記撮像領域１４の画素列方向に形成された複数の垂直信号線VLINと、前記撮像領域１４の画素行方向に形成され、画素行単位で各画素セル１３の光電変換信号を前記複数の垂直信号線VLINに読み出すように制御するための複数の読み出し制御用垂直選択線６と、前記複数の読み出し制御用垂直選択線６を読み出しのタイミングで走査的に選択制御するための第１の垂直選択回路（読み出し用垂直シフトレジスタ）２と、前記垂直信号線VLINを選択するための水平選択トランジスタＴＨと、前記水平選択トランジスタを選択制御するための水平選択回路（水平選択シフトレジスタ）３と、前記水平選択シフトレジスタ３により選択された前記垂直信号線VLINの信号を読み出すための水平信号線HLINと、前記水平信号線HLINに読み出された信号を出力するための出力増幅回路AMP とを具備している。

【００３６】なお、特に図示していないが、図１２に示されるような負荷トランジスタやノイズキャンセラ回路などを撮像領域１４の周辺に備える点は、実施例１のＣＭＯＳ固体撮像装置と同様である。

【００３７】さらに、前記複数の読み出し制御用垂直選択線６を信号蓄積のタイミングで走査的に選択制御するための第２の垂直選択回路（電子シャッタ用垂直シフトレジスタ）１５と、前記第１の垂直選択回路の出力および第２の垂直選択回路の出力に基づいて前記複数の読み出し制御用垂直選択線６を選択的に駆動するための駆動信号を生成する垂直駆動回路（図示せず）とを具備する。

【００３８】即ち、読み出し用の垂直シフトレジスタ２とは別に電子シャッタ用の垂直シフトレジスタ１５が設けられており、この電子シャッタ用垂直シフトレジスタ１５も所定のタイミングで読み出し用垂直シフトレジス

タ2と同様に選択対象行を走査するように構成されている。

【0039】これにより、読み出し用の垂直シフトレジスタ2および電子シャッタ用垂直シフトレジスタ15により、1フィールド期間内に2回のタイミングで特定の選択対象行を選択制御することが可能になる。

【0040】したがって、読み出し用垂直シフトレジスタ2が選択対象行を選択制御して画素信号を垂直信号線VLINに読み出すより前に、電子シャッタ用垂直シフトレジスタ15が選択対象行を選択制御して画素信号の蓄積を開始することにより、等価的に受光時間を制御する電子シャッタ動作が可能になる。

【0041】ところで、上記したような1個の読み出し用垂直シフトレジスタ2および1個の電子シャッタ用垂直シフトレジスタ15を有する図15のCMOS固体撮像装置は、例えば受光センサの出力レベルに応じて自動的に信号蓄積時間を変化させることによって等価的に受光時間を変化させる可変電子シャッタ動作を行わせる場合に、信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じたり、2つの垂直シフトレジスタ2、15の負荷が変動するという問題がある。

【0042】この問題について、以下に説明する。

【0043】図16は、図15中の2つの垂直シフトレジスタ2、15の行選択タイミングが固定である場合の一例を示す。

【0044】図16に示すように、電子シャッタ用垂直シフトレジスタ15が読み出し用垂直シフトレジスタ2よりも先に行選択を行うタイミングが固定されている、つまり、上記2つの垂直シフトレジスタ2、15が行選択を行う時間差は常に一定である。

【0045】このように2つの垂直シフトレジスタ2、15の行選択タイミングが固定であった場合には、読み出し用垂直シフトレジスタ2および電子シャッタ用垂直シフトレジスタ15は、あるフレームの選択を始めて初段から終段まで（つまり、固体撮像装置の垂直方向の画素数）のシフト動作が終わると再び初段に戻り、次のフレームの選択を始める。

【0046】したがって、図15の固体撮像装置は、例えば受光センサの出力レベルに応じて自動的に信号蓄積時間を変化させることによって等価的に受光時間を変化させる可変電子シャッタ動作を行わせる場合に、信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じたり、2つの垂直シフトレジスタ2、15の負荷が変動するという問題がある。

【0047】ここで、信号蓄積時間を変化させるための具体的な手法として、電子シャッタ用垂直シフトレジスタ15が読み出し用垂直シフトレジスタ2よりも先に行選択を行うタイミング（電子シャッタのタイミング）を変化させて画素信号の蓄積を行う時間の長短を変化させる場合について、図17を参照しながら前記問題について詳細に述べる。

【0048】図17において、読み出し制御パルスは読み出し用垂直シフトレジスタ2のシフト動作を開始させる信号であり、可変電子シャッタ制御パルスは電子シャッタ用垂直シフトレジスタ15のシフト動作を開始させる信号である。

【0049】（1）第1のフレームの選択に際して図17中のタイミングt1で発生した電子シャッタの制御パルスにより電子シャッタ用垂直シフトレジスタ15のシフト動作を開始した後、終段までのシフト動作が終わる前（全ての画素行を選択する前）に、図17中のタイミングt3で第2のフレームを選択するために電子シャッタパルスが発生したとする。この場合、電子シャッタ用垂直シフトレジスタ15は上記タイミングt3でリセットされ、再び初段からシフト動作（行選択）を開始する。

【0050】これにより、図17中のタイミングt2で発生した読み出し制御パルスにより読み出し用垂直シフトレジスタ2のシフト動作が開始して前記第1のフレームの読み出しを行う際、前記タイミングt1でシフト動作が開始した電子シャッタ用垂直シフトレジスタ15によって選択指定された画素行と選択指定されなかった画素行とでは信号蓄積時間の差が生じる。

【0051】このように信号蓄積時間の差が生じると、読み出し出力レベルが画素行の位置に依存して変動し、固体撮像装置の出力信号を画像表示装置の画面に表示した場合に横筋などの画像ノイズが発生する原因となる。

【0052】（2）図17中のタイミングt4では、前記タイミングt3でシフト動作が開始した電子シャッタ用垂直シフトレジスタ15の選択行と前記タイミングt2でシフト動作が開始した読み出し用垂直シフトレジスタ2の選択行の計2本の画素行が選択されるので、この2本の画素行が2つの垂直シフトレジスタ2、15の負荷となる。

【0053】これに対して、図17中のタイミングt6では、前記タイミングt3でシフト動作が開始した電子シャッタ用垂直シフトレジスタ15による選択行は既に存在せず、図17中のタイミングt5でシフト動作が開始した読み出し用垂直シフトレジスタ2により1本の画素行が選択されるので、この1本の画素行が2つの垂直シフトレジスタ2、15の負荷となる。

【0054】このように2つの垂直シフトレジスタ2、15の負荷が電子シャッタタイミングに依存して変動すると、固体撮像装置の電源ラインの電圧変動をまねき、固体撮像装置の出力信号を画像表示装置の画面に表示した場合に横筋が発生し、顕著に画質を悪くする原因となる。

【0055】なお、上記したような信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じたり、2つの垂直シフトレジスタ2、15の負荷が変動するという問題は、CMOS型の固体撮像装置に限らず、CCD型

の固体撮像装置で可変電子シャッタ動作を行わせる場合にも生じる。

【0056】

【発明が解決しようとする課題】上記したように従来の固体撮像装置は、信号蓄積時間を変化させて可変電子シャッタ動作を行わせる場合に信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じたり、読み出し用垂直シフトレジスタと電子シャッタ用垂直シフトレジスタの負荷が変動し、出力信号の表示画面に横筋などの画像ノイズが発生する原因となるという問題があった。

【0057】本発明は上記の問題点を解決すべくなされたもので、電子シャッタ動作を行わせる場合に読み出し用垂直シフトレジスタと電子シャッタ用垂直シフトレジスタの負荷の変動を防止でき、出力信号の表示画面における横筋などの画像ノイズの発生を防止し得る固体撮像装置を提供することを目的とする。

【0058】また、本発明は、フィールド単位で画素の信号蓄積時間を変化させる可変電子シャッタ動作（連続電子シャッタ動作）を行わせる場合に読み出し用垂直シフトレジスタと電子シャッタ用垂直シフトレジスタの負荷の変動を防止でき、出力信号の表示画面における横筋などの画像ノイズの発生を防止し得る固体撮像装置を提供することを目的とする。

【0059】また、本発明は、連続電子シャッタ動作を行わせる場合に信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じることを防止し得る固体撮像装置を提供することを目的とする。

【0060】また、本発明は、連続電子シャッタ動作を行わせる場合に、出力信号の表示画面における横筋などの画像ノイズの発生を防止し得る固体撮像装置を提供することを目的とする。

【0061】また、本発明は、画素で光電変換・蓄積された信号を読み出す際に、画素周辺の配線から容量結合によりノイズが飛び込むことを防止し得る固体撮像装置を提供することを目的とする。

【0062】

【課題を解決するための手段】本発明の第１の固体撮像装置は、画素に対する入射光を光電変換して電荷を蓄積する光電変換手段、蓄積した電荷を検出部に読み出す読み出し手段、読み出された電荷を増幅する増幅手段、前記検出部の電荷をリセットするためのリセット手段および前記増幅手段から信号を出力させる垂直選択手段を有する単位セルが半導体基板上に二次元的に配置されてなり、複数の信号読み出し用の画素行および少なくとも２つのダミー画素行を有する撮像領域と、前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各読み出し手段を駆動するための読み出し駆動信号を伝送するための複数本の読取り線と、前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各垂直選択手段を駆動するための行選択駆動信号を伝送するための複数本の垂直選択線と、前記複数本の読取り線に読み出し駆動信号を選択的に供給して前記読み出し手段を駆動するとともに、前記複数本の垂直選択線に行選択駆動信号を選択的に供給して前記垂直選択手段を駆動するための垂直駆動手段と、前記撮像領域における各画素行の読み出し手段を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に２回駆動させるように前記垂直駆動手段を制御する行選択手段と、前記撮像領域における各画素列に対応して設けられ、前記垂直駆動手段により順次駆動された画素行の各単位セルからそれぞれ出力される信号を垂直方向に伝送するための複数の垂直信号線とを具備し、前記行選択手段は、前記垂直駆動手段により前記複数の信号読み出し用の画素行の単位セルからの信号読み出しを制御した後、前記２つのダミー画素行のうちの第１のダミー画素行を駆動させるように選択制御し、前記垂直駆動手段により前記複数の信号読み出し用の画素行の単位セルにおける信号蓄積を制御した後、前記前記２つのダミー画素行のうちの第２のダミー画素行を駆動させるように選択制御することを特徴とする。

【0063】本発明の第２の固体撮像装置は、画素に対する入射光を光電変換して電荷を蓄積する光電変換手段、蓄積した電荷を検出部に読み出す読み出し手段、読み出された電荷を増幅する増幅手段、前記検出部の電荷をリセットするためのリセット手段および前記増幅手段から信号を出力させる垂直選択手段を有する単位セルが半導体基板上に二次元的に配置されてなり、複数の画素行を有する撮像領域と、前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各読み出し手段を駆動するための読み出し駆動信号を伝送するための複数本の読取り線と、前記撮像領域における各画素行に対応して水平方向に設けられ、それぞれ対応する画素行の単位セルの各垂直選択手段を駆動するための行選択駆動信号を伝送するための複数本の垂直選択線と、前記複数本の読取り線に読み出し駆動信号を選択的に供給して前記読み出し手段を駆動するとともに、前記複数本の垂直選択線に行選択駆動信号を選択的に供給して前記垂直選択手段を駆動するための垂直駆動手段と、前記撮像領域における各画素行の読み出し手段を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に２回駆動させるように前記垂直駆動手段を制御する行選択手段と、前記撮像領域における各画素列に対応して設けられ、前記垂直駆動手段により順次駆動された画素行の各単位セルからそれぞれ出力される信号を垂直方向に伝送するための複数の垂直信号線とを具備し、前記行選択手段は、前記垂直駆動手段により前記信号読み出しタイミングで前記各画素行の読み出し手段を駆動させる第１の手段と、前記垂直駆動手段により前記信号蓄積タイミングで前記各画素行の読み出し手

段を駆動させる少なくとも２個の第２の手段とを具備することを特徴とする。

【００６４】本発明の第３の固体撮像装置は、前記第２の固体撮像装置において、前記撮像領域は、信号読み出し用の前記複数の画素行のほかに少なくとも３本のダミー画素行をさらに具備し、前記行選択手段は、前記第１の手段により前記ダミー画素行のうちの１つのダミー画素行を駆動させ、前記２個の第２の手段により前記ダミー画素行のうちの他の２つのダミー画素行を駆動させることを特徴とする。

【００６５】本発明の第４の固体撮像装置は、前記第２または第３の固体撮像装置において、前記行選択手段は、各画素行の信号読み出しタイミングの周期に対応する１フィールド単位で１フィールド周期の期間内における信号蓄積タイミングを変化させることを特徴とする。

【００６６】本発明の第５の固体撮像装置は、前記第４の固体撮像装置において、前記少なくとも２個の第２の手段は、互いに前記信号読み出しタイミングに対する信号蓄積タイミングを相対的に異ならせて前記読み出し手段を駆動させるものであり、前記第２の手段による前記垂直駆動手段の制御動作が１フィールド毎に交互に切換えられることを特徴とする。

【００６７】本発明の第６の固体撮像装置は、前記第１乃至第５のいずれか１つの固体撮像装置において、前記行選択手段は、前記撮像領域における各画素行の読み出し手段を２回駆動させる際、前記光電変換手段の周辺で前記読取り線に隣接する他の配線の電圧を前記２回の駆動時とも実質的に同一にするように前記垂直駆動手段を制御することを特徴とする。

【００６８】本発明の第７の固体撮像装置は、半導体基板上の撮像領域に二次元的に配置された単位セルの光電変換素子から蓄積電荷を読み出す際、この読み出しを制御する配線を所望の信号蓄積タイミングおよび信号読み出しタイミングで順次に２回駆動させ、前記信号読み出しタイミングで読み出された信号を出力させる電子シャッタ動作を行う固体撮像装置において、前記読み出しを制御する配線に隣接し、前記光電変換素子の周辺に存在する他の配線の電圧を前記信号蓄積タイミングと信号読み出しタイミングとで実質的に同一にすることを特徴とする。

【００６９】本発明の第８の固体撮像装置は、２画素／１ユニットの単位セルが半導体基板上に二次元的に配置されてなる撮像領域を有する固体撮像装置において、前記撮像領域の単位セルにおける２画素の光電変換素子からそれぞれ蓄積電荷を読み出す際、この読み出しを制御する配線に隣接し、前記光電変換素子の周辺に存在する他の配線の電圧を各画素の読み出し時に実質的に同一にすることを特徴とする。

【００７０】

【発明の実施の形態】以下、図面を参照して本発明の実施の形態を詳細に説明する。

【００７１】<第１の実施の形態>図１は、第１の実施の形態の増幅型ＣＭＯＳ固体撮像装置の等価回路を示している。

【００７２】図１のＣＭＯＳ固体撮像装置は、図１５を参照して前述した従来例２のＣＭＯＳ固体撮像装置と比べて、大部分は同様であるが、読み出し用の垂直シフトレジスタ２ａおよび電子シャッタ用の垂直シフトレジスタ１５ａなどが異なり、その他は同じであるので図１５中と同一符号を付している。

【００７３】即ち、図１のＣＭＯＳ固体撮像装置は、例えば図１２の従来例１で示したように構成される画素セル１３が行列状に二次元的に配置された撮像領域（光電変換部）１４と、前記撮像領域１４の画素列方向に形成された複数の垂直信号線VLINと、前記撮像領域１４の画素行方向に形成され、画素行単位で各画素セル１３の光電変換信号を前記複数の垂直信号線VLINに読み出すように制御するための複数の読み出し制御用垂直選択線６と、前記複数の読み出し制御用垂直選択線６を読み出しのタイミングで走査的に選択制御するための第１の垂直選択回路（読み出し用垂直シフトレジスタ）２ａと、前記複数の読み出し制御用垂直選択線６を信号蓄積のタイミングで走査的に選択制御するための第２の垂直選択回路（電子シャッタ用垂直シフトレジスタ）１５ａと、前記第１の垂直選択回路２ａの出力および第２の垂直選択回路１５ａの出力に基づいて前記複数の読み出し制御用垂直選択線６を選択的に駆動するための駆動信号を生成する垂直駆動回路（パルスセレクタ）１６と、前記垂直信号線VLINを選択するための水平選択トランジスタＴＨと、前記水平選択トランジスタＴＨを選択制御するための水平選択回路（水平選択シフトレジスタ）３と、前記水平選択シフトレジスタ３により選択された前記垂直信号線VLINの信号を読み出すための水平信号線HLINと、前記水平信号線HLINに読み出された信号を出力するための出力増幅回路AMP とを具備している。

【００７４】なお、図１５の従来例２のＣＭＯＳ固体撮像装置と同様に、ここでは特に図示されていないが、図１２に示されるような負荷トランジスタやノイズキャンセラ回路などを撮像領域１４の周辺に備えている。

【００７５】そして、さらに、

（１）前記撮像領域１４に本来の画素行とは別に２本のダミー画素行（第１のダミー画素行１４１および第２のダミー画素行１４２）が付加されている。（２）前記読み出し用の垂直シフトレジスタ（第１の垂直シフトレジスタ）２ａは、撮像領域１４の本来の画素行数＋１のシフト段数を有し、前記電子シャッタ用の垂直シフトレジスタ（第２の垂直シフトレジスタ）１５ａも、撮像領域１４の本来の画素行数＋１のシフト段数を有する。

（３）垂直駆動回路１６は、読み出し用の垂直シフトレジスタ２ａの最終段出力信号を選択して前記第１のダミ

一画素行１４１に供給し、電子シャッタ用の垂直シフトレジスタ１５ａの最終段出力信号を選択して前記第２のダミー画素行１４２に供給するように構成されている。

【００７６】前記２本のダミー画素行１４１、１４２は、本来の画素行と同じ構成であるが、垂直駆動回路１６により選択された時に負荷として作用するために付加されたものである。

【００７７】図１の固体撮像装置においては、電子シャッタ用の垂直シフトレジスタ１５ａおよび読み出し用の垂直シフトレジスタ２ａにより、同じ垂直選択線を１フィールド期間内に２回選択制御することが可能であり、画素（フォトダイオード）の信号蓄積時間を制御するシャッタ動作を行うことができる。

【００７８】この場合、電子シャッタ用の垂直シフトレジスタ１５ａは、信号蓄積の開始タイミングを制御するシフトクロック信号に基づいてシフト動作を行い、シャッタ動作期間には各対応する画素行を選択制御して画素の信号蓄積を行わせる（読み出しは行わない）ように制御し、シャッタ動作期間以外（画素行の選択終了後から次回の選択開始までの期間）は第２のダミー画素行１４２を選択制御する。

【００７９】また、読み出し用の垂直シフトレジスタ２ａは、信号読み出しの開始タイミングを制御するシフトクロック信号に基づいてシフト動作を行い、垂直期間内の垂直有効走査期間における各水平期間には各対応する画素行を選択制御し、垂直帰線期間には第１のダミー画素行１４１を選択制御する。

【００８０】即ち、上記第１の実施の形態の固体撮像装置によれば、垂直駆動回路１６は、読み出し用の垂直シフトレジスタ２ａおよび電子シャッタ用の垂直シフトレジスタ１５ａの各出力にそれぞれ対応して１本ずつ（合計２本）の画素行を常に選択駆動しており、常に選択負荷が等しいので、選択負荷の大小による読み出しレベルの変動に起因する表示画面上の横縞の発生を防ぐことができる。

【００８１】＜第２の実施の形態＞図２は、第２の実施の形態の増幅型ＣＭＯＳ固体撮像装置の等価回路を示している。

【００８２】図２のＣＭＯＳ固体撮像装置は、図１を参照して前述した第１の実施の形態のＣＭＯＳ固体撮像装置に対して、（１）前記撮像領域１４にさらに１本のダミー画素行（第３のダミー画素行１４３）が追加されている点、（２）さらに、電子シャッタ用の垂直シフトレジスタ１５ａと同じシフト段数を有する１個の電子シャッタ用の垂直シフトレジスタ１５ｂが追加され、その各段出力が前記電子シャッタ用の垂直シフトレジスタ１５ａの各段出力とフィールド単位で切り換え選択されて垂直駆動回路（パルスセレクタ）１６ａで使用される点、（３）垂直駆動回路１６ａは、３個の垂直シフトレジスタ２ａ、１５ａ、１５ｂの出力に基づいて前記複数の読み出し制御用垂直選択線６を選択的に駆動するための駆動信号を生成する点、（４）垂直駆動回路１６ａは、追加された電子シャッタ用の垂直シフトレジスタ１５ｂの最終段出力信号を選択して前記第３のダミー画素行１４３に供給する点が若干異なり、その他は同じであるので図１中と同一符号を付している。

【００８３】図３は、図２の固体撮像装置において２個の電子シャッタ用垂直シフトレジスタ１５ａ、１５ｂがフィールド単位で交互に電子シャッタ動作を制御する様子を示すタイミング図である。

【００８４】図３に示すタイミング図から分かるように、図２の固体撮像装置においては、電子シャッタ専用の２個の垂直シフトレジスタ１５ａ、１５ｂのシフト動作をフィールド単位で交互に開始させ、それぞれの出力をフィールド単位で交互に選択することにより、電子シャッタ動作をフィールド単位で交互に電子シャッタ専用の２個の垂直シフトレジスタ１５ａ、１５ｂに振り分けている。

【００８５】この場合、選択された電子シャッタ専用の垂直シフトレジスタ１５ａ、１５ｂは、読み出し用垂直シフトレジスタ２ａよりも先に行選択を行うものであり、そのタイミングを変化させることにより画素信号の蓄積を行う時間の長短を変化させることが可能になる。

【００８６】したがって、電子シャッタ用の垂直シフトレジスタ１５ａ、１５ｂおよび読み出し用の垂直シフトレジスタ２により同一垂直ラインを１フィールド期間に２回選択し、選択画素の信号蓄積時間を制御する可変電子シャッタ動作を行うことができる。

【００８７】また、電子シャッタ制御信号がフィールド周期より短い時間間隔で入力されたとしても、既にシフト動作を開始している一方の電子シャッタ専用の垂直シフトレジスタ１５ａまたは１５ｂのシフト動作が最終段に達する前（読み出し用の全ての画素行の選択を終わらないうち）に途中でリセットされることなく、最後の画素行まで順次選択して選択画素の信号蓄積時間を制御する。

【００８８】そして、読み出し用画素行の最終行の選択終了後から次々回のフィールド期間における１行目の読み出し用画素行の選択開始までの期間は第２のダミー画素行１４２あるいは第３のダミー画素行１４３を選択制御する。

【００８９】また、読み出し用の垂直シフトレジスタ２ａは、垂直有効走査期間内の各水平期間には各対応する画素行を選択制御し、垂直帰線期間には第１のダミー画素行１４１を選択制御する。

【００９０】つまり、各垂直シフトレジスタ２ａ、１５ａ、１５ｂは、それぞれ全ての読み出し用の画素行を選択した後もダミー画素行を選択し続け、後のフィールド期間における選択開始を待機する。

【００９１】即ち、上記第２の実施の形態の固体撮像装

置によれば、フィールド単位で交互に電子シャッタ専用の2個の垂直シフトレジスタに電子シャッタ動作を振り分けることにより、フィールド間で信号蓄積時間を変化させることが可能になる。

【0092】この場合、読み出しの走査時間は一定のままで、信号蓄積時間をフィールド単位で連続的に変化させる電子シャッタ機能を実現することが可能になる。なお、同一フィールド内では、どの選択画素行も信号蓄積時間は同じである。

【0093】このように信号蓄積時間を変化させて可変電子シャッタ動作を行わせる場合に、信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じることを防止でき、出力信号の表示画面における横筋などの画像ノイズの発生を防止することができる。

【0094】また、垂直駆動回路16aは、読み出し用の垂直シフトレジスタ2aおよび2個の電子シャッタ用の垂直シフトレジスタ15a、15bの各出力にそれぞれ対応して1本ずつ（合計3本）の画素行を常に選択駆動しており、常に選択負荷が等しいので、選択負荷の大小による読み出しレベルの変動に起因する表示画面上の横縞の発生を防ぐことができる。

【0095】なお、図1および図2に示した固体撮像装置は、1画素毎に画素信号の読み出しが可能な読み出し回路を備えたCMOS型の固体撮像装置に限らず、水平信号線単位で読み出しを行うCCD（電荷結合デバイス）型の固体撮像装置にも適用可能である。

【0096】<第3の実施の形態>図4は、第3の実施の形態の増幅型CMOS固体撮像装置の等価回路を示している。

【0097】図4のCMOS固体撮像装置は、図12を参照して前述した従来例1のCMOS固体撮像装置に対して、例えば受光センサの出力レベルに応じて自動的に信号蓄積時間を変化させることによって等価的に受光時間を変化させる可変電子シャッタ動作をフィールド単位で連続的に変化させることが可能になるように工夫がなされている。

【0098】即ち、図4のCMOS固体撮像装置は、図12を参照して前述した従来例1のCMOS固体撮像装置と比べて、大部分は同様であるが、（1）読み出し用の垂直シフトレジスタ2とは別に2個の電子シャッタ用の垂直シフトレジスタ21、22が付加されている点、（3）2個の電子シャッタ用の垂直シフトレジスタ21、22の動作（信号蓄積時間の制御パルスの出力動作）をフィールド単位で交互に切り換え制御するためのレジスタ切換制御回路（SEL）23が付加されている点、（4）タイミング発生回路10aおよびパルスセレクタ回路24の構成が異なり、その他は同じであるので図12中と同一符号を付している。

【0099】即ち、図4において、セル領域（撮像領域）には、例えば4個のトランジスタTa、Tb、Tc、Tdと、1個のフォトダイオードPDから構成される1ピクセル（1画素）／1ユニットの単位セルが二次元の行列状に配置されて形成されている。この場合、各単位セルは、アノード側に接地電位が与えられるフォトダイオードPDと、フォトダイオードPDのカソード側に一端側が接続されている読み出しトランジスタ（シャッタゲートトランジスタ）Tdと、読み出しトランジスタTdの他端側にゲートが接続されている増幅トランジスタTbと、増幅トランジスタTbの一端側に一端側が接続されている垂直選択トランジスタ（行選択トランジスタ）Taと、増幅トランジスタTbのゲートに一端側が接続されているリセットトランジスタTcとを具備する。

【0100】そして、前記セル領域には、各画素行に対応して、同一行の単位セルの各読み出しトランジスタTdのゲートに共通に接続された複数の読取り線4と、同一行の単位セルの各垂直選択トランジスタTaのゲートに共通に接続された垂直選択線6と、同一行の単位セルの各リセットトランジスタTcのゲートに共通に接続されたリセット線7が形成されている。

【0101】また、前記セル領域には、各画素列に対応して、同一列の単位セルの各増幅トランジスタTbの他端側に共通に接続された垂直信号線VLINと、同一列の単位セルの各リセットトランジスタTcの他端側および各垂直選択トランジスタTaの他端側に共通に接続された電源線9が形成されている。

【0102】さらに、セル領域の一端側の外部には、前記垂直信号線VLINの各一端側と接地ノードとの間にそれぞれ接続された複数の負荷トランジスタTLが水平方向に配置されている。

【0103】また、セル領域の他端側の外部には、例えば2個のトランジスタTSH、TCLPと2個のコンデンサCc、Ctから構成された複数のノイズキャンセラ回路が水平方向に配置されている。

【0104】そして、上記各ノイズキャンセラ回路を介して前記垂直信号線VLINの各他端側に接続された複数の水平選択トランジスタTHが水平方向に配置されている。

【0105】上記水平選択トランジスタTHの各他端に共通に水平信号線HLINが接続されており、この水平信号線HLINには水平リセットトランジスタ（図示せず）および出力増幅回路AMP が接続されている。

【0106】なお、前記各ノイズキャンセラ回路は、垂直信号線VLINの他端側に一端側が接続されたサンプルホールド用のトランジスタTSHと、このサンプルホールド用のトランジスタTSHの他端側に一端側が接続された結合コンデンサCcと、この結合コンデンサCcの他端側と接地ノードとの間に接続された電荷蓄積用のコンデンサCtと、前記コンデンサCc、Ctの接続ノードに接続された電位クランプ用のトランジスタTCLPとにより構

成されており、前記コンデンサＣｃ、Ｃｔの接続ノードに前記水平選択トランジスタＴＨの一端側が接続されている。

【０１０７】さらに、セル領域の外部には、セル領域の複数の垂直選択線６を走査的に選択制御するための読み出し用の垂直シフトレジスタ２と２個の電子シャッタ用の垂直シフトレジスタ（ＥＳ１）２１および（ＥＳ２）２２、上記３個の垂直シフトレジスタ２、２１、２２の出力パルスを選択制御してセル領域の各行の垂直選択線６を走査的に駆動するためのパルスセレクタ２４、前記複数の水平選択トランジスタＴＨを走査的に駆動するための水平シフトレジスタ３、前記２個の電子シャッタ用の垂直シフトレジスタ２１、２２の動作（信号蓄積時間の制御パルスの出力動作）をフィールド単位で交互に切り換え制御するためのレジスタ切換制御回路２３、各種のタイミング信号を発生するタイミング発生回路１０ａ、前記ノイズキャンセラ回路の電位クランプ用のトランジスタTCLPの一端などに所定のバイアス電位を発生するためのバイアス発生回路１１がそれぞれ配置されている。

【０１０８】前記タイミング発生回路１０ａは、フィールド周期のタイミング信号φＶＲ、フィールド周期で可変設定される蓄積時間制御用のタイミング信号φＥＳ、水平帰線期間に対応するパルス信号φＨＰ、クロックパルス信号φＣＫが入力する。

【０１０９】そして、前記タイミング信号φＶＲ入力をバッファ整形して読み出し用の垂直シフトレジスタに供給するためのタイミング信号φＶＲＲを生成し、前記パルス信号φＨＰ入力をバッファ整形して読み出し用の垂直シフトレジスタおよび２個の電子シャッタ用の垂直シフトレジスタ２１、２２に供給するためのタイミング信号φＨＰＶを生成する。

【０１１０】また、前記パルスセレクタ２４に供給するためのタイミング信号φＲＯＲＥＡＤ、φＥＳＲＥＡＤ、φＲＥＳＥＴ、φＡＤＲＥＳを生成し、前記ノイズキャンセラ回路に供給するためのパルス信号φＣＬＰ、φＳＨを生成する。また、水平シフトレジスタ３に供給するためのパルス信号φＨを生成する。

【０１１１】また、フィールド周期のタイミング信号φＶＲに基づいてフィールド切換制御用のパルス信号φＦＩを生成し、信号蓄積時間制御用のタイミング信号φＥＳＲとともに前記レジスタ切換制御回路２３に供給する。

【０１１２】前記レジスタ切換制御回路２３は、フィールド切換制御用のパルス信号φＦＩ入力に基づいてフィールド単位毎に蓄積時間制御用のタイミング信号φＥＳＲの供給先を交互に切り換える。この場合、前記電子シャッタ用の垂直シフトレジスタ２１に供給する信号蓄積時間制御用のタイミング信号をφＥＳＲ１、前記電子シャッタ用の垂直シフトレジスタ２２に供給する信号蓄積時間制御用のタイミング信号をφＥＳＲ２で表わしている。

【０１１３】図５は、図４中のパルスセレクタ２４の一例を示す回路図である。

【０１１４】図５に示すパルスセレクタは、読み出し用の垂直シフトレジスタの出力信号ＲＯｎ、２個の電子シャッタ用の垂直シフトレジスタ２１、２２の各出力信号ＥＳ１ｎ、ＥＳ２ｎが入力するとともに、前記タイミング発生回路１０ａから供給されるタイミング信号φＲＯＲＥＡＤ、φＥＳＲＥＡＤ、φＲＥＳＥＴ、φＡＤＲＥＳが入力し、これらの入力信号の論理処理を行って各種の駆動信号φＲＥＡＤｎ、φＲＥＳＥＴ、φＡＤＲＥＳｎを出力し、セル領域に供給するように論理ゲートにより構成されている。

【０１１５】即ち、読み出し用の垂直シフトレジスタの出力信号ＲＯｎが活性状態の時にはタイミング信号φＲＯＲＥＡＤを選択して読取り線駆動信号φＲＥＡＤｎとして出力し、２個の電子シャッタ用の垂直シフトレジスタ２１、２２の各出力信号ＥＳ１ｎ、ＥＳ２ｎのいずれかが活性状態の時にはタイミング信号φＥＳＲＥＡＤを選択して読取り線駆動信号φＲＥＡＤｎとして出力する。

【０１１６】また、読み出し用の垂直シフトレジスタの出力信号ＲＯｎ、２個の電子シャッタ用の垂直シフトレジスタ２１、２２の各出力信号ＥＳ１ｎ、ＥＳ２ｎのいずれか１つが活性状態の時には、タイミング信号φＲＥＳＥＴを選択してリセット線駆動信号φＲＥＳＥＴｎとして出力する。

【０１１７】また、読み出し用の垂直シフトレジスタの出力信号ＲＯｎが活性状態の時にはタイミング信号φＡＤＲＥＳを選択して垂直選択線駆動信号φＡＤＲＥＳｎとして出力する。

【０１１８】図６は、図４の固体撮像装置におけるフィールド単位で連続的に変化させることが可能な可変電子シャッタ動作を説明するために、図４中のタイミング発生回路１０ａ、３個の垂直シフトレジスタ２、２１、２２およびパルスセレクタ２４の動作例を示すタイミング波形図である。

【０１１９】ここでは、図４の固体撮像装置が１フィールド＝１／３０Ｈｚ（１フィールドを１フレームとする３０フレーム／秒の画像）の撮像システムで使用される場合を示している。

【０１２０】図６において、φＶＲはフィールド周期のタイミング信号入力、φＥＳはフィールド周期で可変設定される蓄積時間制御用のタイミング信号入力、φＶＲＲは読み出し用の垂直シフトレジスタに供給されるフィールド周期のタイミング信号、φＦＩはフィールド切換制御用のパルス信号、φＥＳＲ１は一方の電子シャッタ用の垂直シフトレジスタ２１に１フィールドおきに供給される蓄積時間制御用のタイミング信号、φＥＳＲ２は

他方の電子シャッタ用の垂直シフトレジスタ２２に１フィールド間隔で供給される蓄積時間制御用のタイミング信号、ＲＯ(i)は読み出し用の垂直シフトレジスタＲＯの出力、ＥＳ１(i) は一方の電子シャッタ用の垂直シフトレジスタ２１の出力、ＥＳ２(i) は他方の電子シャッタ用の垂直シフトレジスタ２２の出力である。

【０１２１】図７は、図６中の１フィールド期間内の電子シャッタ動作の一例を示すタイミング波形図である。

【０１２２】図７において、ＥＳｎは電子シャッタ用の垂直シフトレジスタ２１あるいは２２のｎ段目の出力信号、ＲＯｎは読み出し用の垂直シフトレジスタ２のｎ段目の出力信号である。

【０１２３】ｔＨＥＳは、電子シャッタ用の垂直シフトレジスタ２１あるいは２２のｎ段目の出力信号ＥＳｎが活性状態（“Ｈ”レベル）になる１水平期間を示す。

【０１２４】ｔＨＲＯは、読み出し用の垂直シフトレジスタ２のｎ段目の出力信号ＲＯｎが活性状態（“Ｈ”レベル）になる１水平期間を示す。

【０１２５】ＨＢＬＫは、１水平期間を水平帰線期間と水平有効走査期間とに分けるための制御パルス信号である。

【０１２６】φＣＬＰおよびφＳＨはノイズキャンセラ回路に供給されるパルス信号であり、それぞれ水平帰線期間毎に生成される。

【０１２７】φＨは水平選択トランジスタＴＨに供給されるパルス信号であり、水平有効走査線期間内で水平方向に配置された水平選択トランジスタＴＨが順次オンになるように生成される。

【０１２８】φＡＤＲＥＳ、φＲＥＳＥＴおよびφＲＥＡＤは、前記パルスセレクタ２４から選択画素行に供給されるパルス信号であり、そのうちのφＲＥＳＥＴ、φＲＥＡＤは、それぞれ信号蓄積動作および信号読み出し動作の際に水平帰線期間内に活性化されるが、φＡＤＲＥＳは、信号蓄積動作の際には生成されず、信号読み出し動作の際に水平帰線期間内に活性化される。

【０１２９】この場合、上記パルス信号φＡＤＲＥＳは、後述するような理由により、信号読み出し動作の際の水平帰線期間内に同一行の垂直選択線６を２回選択制御するように、断続的に２回活性状態になるように生成される。

【０１３０】次に、図６および図７を参照しながら、図４の固体撮像装置の動作を説明する。

【０１３１】図４の固体撮像装置の動作は、前述した従来例１の固体撮像装置（図１２）の動作（図１３）と比べて、基本的には同じであるので同じ動作の説明は省略し、以下、主として異なる動作について説明する。

【０１３２】即ち、図４の固体撮像装置は、電子シャッタ動作を行う際、レジスタ切換制御回路２３により２個の電子シャッタ用の垂直シフトレジスタ２１、２２のシフト動作をフィールド単位で交互に開始させ、それぞれの出力をフィールド単位で交互に選択することにより、電子シャッタ動作をフィールド単位で交互に電子シャッタ専用の２個の垂直シフトレジスタ２１、２２に振り分ける。

【０１３３】これにより、図６中のフィールド期間ｔＦａ、ｔＦｂに示すように、信号蓄積時間制御用のタイミング信号φＥＳがフィールド周期より短い時間間隔で入力されたとしても、電子シャッタ専用の垂直シフトレジスタ２１および２２が同時に動作することが可能になる。

【０１３４】この場合、最初に発生するタイミング信号φＥＳＲ１あるいはφＥＳＲ２により既にシフト動作を開始している一方の電子シャッタ専用の垂直シフトレジスタ２１あるいは２２のシフト動作が読み出し用の全ての画素行の選択制御を終わらないうちに途中でリセットされることなく、読み出し用の画素行の最後まで順次選択して選択画素の信号蓄積時間を制御することが可能になる。

【０１３５】換言すれば、読み出しの走査時間は一定のままで、信号蓄積時間をフィールド単位で連続的に変化させる電子シャッタ機能（連続電子シャッター動作）を実現することが可能になる。なお、同一フィールド内では、どの選択画素行も信号蓄積時間は同じである。

【０１３６】また、図７に示すように、前記水平期間ｔＨＥＳに電子シャッタ用の垂直シフトレジスタのｎ段目のシフト段の出力信号ＥＳｎにより選択制御したｎ行目の画素行にパルス信号φＲＥＳＥＴとφＲＥＡＤが供給され、このｎ行目の画素行のフォトダイオードＰＤでそれ以前に蓄積していた信号電荷を増幅用トランジスタのゲートに読み出すことによって、フォトダイオードの信号電荷を零にする。

【０１３７】この場合、パルス信号φＡＤＲＥＳが“Ｌ”のままであり、垂直選択用トランジスタはオフのままであるので、前記増幅用トランジスタのゲートに読み出された信号電荷は垂直信号線ＶＬＩＮへは出力されない。

【０１３８】この後、前記画素行からの信号読み出し動作の際に、前記水平期間ｔＨＲＯにおける水平帰線期間にφＲＥＳＥＴが一時的に活性化した後、φＡＤＲＥＳが活性化し、さらにφＲＥＡＤが一時的に活性化する。

【０１３９】この場合、前記φＲＥＡＤが活性状態（“Ｈ”レベル）の時に、フォトダイオードとその周辺配線（本例では後述するφＡＤＲＥＳ配線）との間の容量結合の影響によるノイズの飛び込みが発生しないように、φＡＤＲＥＳパルスを信号蓄積動作時と同じ状態となるように一時的に非活性状態（“Ｌ”レベル）にし、このφＡＤＲＥＳが非活性状態の期間内に前記φＲＥＡＤを一時的に活性化している。

【０１４０】このような前記水平期間ｔＨＲＯにおける水平帰線期間内における信号読み出し時の動作を詳しく

説明すると、まず、φRESETによって増幅トランジスタTbのゲート電極を基準電位にリセットした後、φADRESを活性状態（1回目）にして前記n行目の画素行の垂直選択トランジスタTaをオン状態とし、この活性期間内にノイズキャンセラ回路に供給するパルス信号φCLPを活性化し、黒レベルをクランプする。

【0141】そして、φADRESが非活性状態の期間内にφREADを活性化することによって前記フォトダイオードPDでそれ以前に蓄積していた信号電荷を増幅トランジスタTbのゲートに読み出す。

【0142】そして、φADRESを再び活性状態（2回目）にして前記n行目の画素行の垂直選択トランジスタTaを再びオン状態とし、前記増幅トランジスタTbのゲートに読み出されている信号電荷を垂直信号線VLINへ出力する。

【0143】以上の動作により、前記水平期間tHESにおける読取り線駆動信号φREADの活性状態（“H”レベル）の終了時点から前記水平期間tHROにおける読取り線駆動信号φREADの活性化時点までが信号蓄積時間となる。

【0144】図8（a）は、前記ノイズの飛び込みを説明するために、撮像領域の単位セルの一部を取り出して示す平面図である。

【0145】図8（b）は、同図（a）のa－a´線に沿う断面図である。

【0146】図8（c）および（d）は、それぞれ対応して同図（a）中のφADRESが“L”レベルの時／“H”レベルの時にφREADが活性化して信号電荷を読み出す場合の基板内の電位ポテンシャルを示す。ここでは、電源電位が例えば3．3Vである場合を示している。

【0147】図8（a）、（b）において、81はシリコン基板の表層部に形成されたP型ウエル領域、82は基板表層部に選択的に形成された素子分離領域（例えばLOCOS領域）である。基板表層部の素子領域には、フォトダイオードのカソード領域および読み出しトランジスタTdのソース領域を兼ねるn型領域と、読み出しトランジスタTdのドレイン領域となるn型領域（検出ノードDN）が選択的に形成されている。

【0148】上記読み出しトランジスタTdのチャネル領域上には絶縁ゲート膜を介してポリシリコン配線からなるゲート電極（読取り線4の一部）が形成されており、フォトダイオードPDのn型領域の近傍の素子分離領域82上にはポリシリコン配線からなる垂直選択線5およびリセット線7が略平行に形成されている。

【0149】本実施の形態の読み出し動作に際しては、図8（c）に示すように、フォトダイオードPDに隣接するφADRES配線が“L”レベルの時にφREADが活性化して信号電荷を読み出すので、フォトダイオードPDとφADRES配線との間に存在する結合容量Caによりフォトダイオード PD下の基板内の電位ポテンシャルが－VCaだけ引き下げられ、フォトダイオードPDの蓄積電荷QCaが読み出される。

【0150】これに対して、図8（d）に示すように、フォトダイオードPDに隣接するφADRES配線が“H”レベルの時にφREADが活性化して信号電荷を読み出すと、フォトダイオードPDとφADRES配線との間に存在する結合容量Caによりフォトダイオード PD下の基板内の電位ポテンシャルが＋VCaだけ引き上げられる（ノイズの飛び込みとなる）ので、フォトダイオードPDの蓄積電荷QCa分が読み出されなくなり、固体撮像装置の出力信号を画像表示装置の画面に表示した場合に黒信号がつぶれて見苦しい画像になる。

【0151】なお、上記第3の実施の形態の固体撮像装置においても、前記第2の実施の形態の固体撮像装置と同様に、（1）前記撮像領域に第1～第3のダミー画素行を追加し、（2）3個の垂直選択回路2、21、22のシフト段数を本来の撮像用の画素行数＋1の段数とし、（3）垂直選択回路2、21、22の出力に基づいて複数の水平方向の制御線群（4、6、7）を選択的に駆動するための駆動信号をパルスセレクタ24で生成する際、垂直選択回路2の最終段出力信号の活性化期間は第1のダミー画素行を選択して駆動し、第2の垂直選択回路21の最終段出力信号の活性化期間は第2のダミー画素行を選択して駆動し、第3の垂直選択回路22の最終段出力信号の活性化期間は第3のダミー画素行を選択して駆動するように構成してもよい。

【0152】このような構成により、パルスセレクタ24は、読み出し用の垂直シフトレジスタ2および2個の電子シャッタ用の垂直シフトレジスタ21、22の各出力にそれぞれ対応して1本ずつ（合計3本）の画素行を常に選択駆動するようになり、常に選択負荷が等しいので、選択負荷の大小による読み出しレベルの変動に起因する表示画面上の横縞の発生を防ぐことが可能になる。

【0153】なお、前記第3の実施の形態では、フォトダイオードPDとの容量結合による黒つぶれの問題が生じる周辺配線としてφADRES配線が存在する場合を説明したが、上記周辺配線としてφRESET配線あるいはその他の配線が存在する場合にも、これらの配線とフォトダイオードPDとの容量結合による黒信号のつぶれ（黒つぶれ）の問題が生じるおそれがあるので、これらの配線に関しても前記第3実施の形態におけるφADRES配線と同様にレベルを制御すればよい。

【0154】即ち、上記したようにフォトダイオードPDに隣接する読み出しゲート配線以外のフォトダイオードPDの周辺配線の印加電圧として、信号読み出し動作時の信号読み出しパルスφREADの活性化期間と電子シャッタ動作時の読み出しパルスφREADの活性化期間に同じ電圧を印加することにより、フォトダイオードPDと周辺配線との容量結合によってフォトダイオード

PDから余分な電荷が読み出されないように制御することができでき、いわゆる黒つぶれのない再生像が得られる。

【0155】なお、本発明は、以下の第4の実施の形態に述べるような2画素／1ユニットの単位セルのアレイを有する固体撮像装置にも前記各実施の形態に準じて適用可能である。

【0156】<第4の実施の形態>図9は、第4の実施の形態の増幅型CMOS固体撮像装置における2画素／1ユニットの単位セルの等価回路を示している。このCMOS固体撮像装置は、単位セルの構成以外は前述した各実施の形態と同様に構成することができるので、以下、主として2画素／1ユニットの単位セルの構成について説明する。

【0157】図9に示す単位セル30は、2個のフォトダイオード31a、31bを有し、この2個のフォトダイオード31a、31bは、各アノード側に接地電位が与えられ、各カソード側はそれぞれ対応して読み出しトランジスタ（シャッタゲートトランジスタ）32a、32bを介して1個の増幅トランジスタ33のゲートに共通に接続される。上記2個の読み出しトランジスタ32a、32bの各ゲートにはそれぞれ読取り線4a、4bが接続されている。

【0158】前記増幅トランジスタ33は、一端側が垂直信号線VLINに接続され、他端側が垂直選択トランジスタ34を介して電源線9に接続（つまり、前記増幅トランジスタ33はソースフォロア接続）されており、上記垂直選択トランジスタ34のゲートには垂直選択線（アドレス線）6が接続されている。

【0159】さらに、前記増幅トランジスタ33のゲートと電源線9との間に1個のリセットトランジスタ35が接続されており、このリセットトランジスタ35のゲートにはリセット線7が接続されている。

【0160】上記構成の2画素／1ユニットの単位セルは撮像領域に二次元の行列状に配置される。そして、前記2本の読取り線（第1の読取り線4aおよび第2の読取り線4b）、垂直選択線（アドレス線）6およびリセット線7は、撮像領域上に水平方向に形成されており、前記垂直信号線VLINおよび電源線9は、撮像領域上に垂直方向に形成されている。

【0161】図10（a）は、図9の2画素／1ユニットの単位セルの平面パターンの一例を示し、そのB－B線に沿う断面構造を図10（b）を概略的に示している。

【0162】図10（a）、（b）において、90はN型シリコン基板であり、その表層部にPウエル91が形成されている。このPウエル91の表層部には、素子分離領域（例えばLOCOS領域）92、一方のフォトダイオード31aのカソード領域および一方の読み出しトランジスタ32aのソース領域となるN型不純物領域93、他方のフォトダイオード31bのカソード領域および他方の読み出しトランジスタ32bのソース領域となるN型不純物領域932およびNMOSトランジスタのSDG領域（図には読み出しトランジスタ32a、32bの共通ドレインとなるN型不純物領域94のみ示す）が選択的に形成されている。

【0163】そして、基板表面上にシリコン酸化膜（ゲート絶縁膜）95が形成され、前記LOCOS領域92の底面下にはフィールドイオンインプラ領域96が形成されている。

【0164】97は増幅トランジスタ33のゲート電極を一部に含むポリシリコンゲート配線、98は増幅トランジスタ33のドレイン領域および垂直選択トランジスタ34のソース領域となるN型不純物領域、99はリセットトランジスタ35のソース領域となるN型不純物領域である。

【0165】100はリセットトランジスタ35のソース領域99と増幅トランジスタ33のゲート配線97と2個の読み出しトランジスタ32a、32bの共通ドレイン領域とを接続する配線である。

【0166】読取り線4aは読み出しトランジスタ32aのゲート電極を一部に含むポリシリコンゲート配線、読取り線4bは読み出しトランジスタ32bのゲート電極を一部に含むポリシリコンゲート配線からなる。

【0167】垂直選択線（アドレス線）6は垂直選択トランジスタ34のゲート電極を一部に含むポリシリコンゲート配線、リセット線7はリセットトランジスタ35のゲート電極を一部に含むポリシリコンゲート配線からなる。

【0168】33aは前記増幅トランジスタ33のソース領域と垂直信号線VLINとのコンタクト部、34aは上記垂直選択トランジスタ34のドレイン領域と電源線9とのコンタクト部である。97aは増幅トランジスタ33のゲート配線97と配線100とのコンタクト部、99aはリセットトランジスタ35のソース領域99と配線100とのコンタクト部、99bはリセットトランジスタ35のドレイン領域と電源線9とのコンタクト部、100aは上記配線100と2個の読み出しトランジスタ32a、32bの共通ドレイン領域とのコンタクト部である。

【0169】上記構成の2画素／1ユニットの単位セルの動作は、前記1画素／1ユニットの単位セルの動作と比べて、5個のトランジスタを所定の順序で動作させてフォトダイオードから信号電荷を読み出す基本動作は同じであるが、2個のフォトダイオード31a、31bから異なるタイミングで信号電荷を読み出す点が異なる。つまり、一方のフォトダイオード31aから信号電荷を読み出す時は第1の読取り線4aに“H”レベルの読取り信号を与え，第2の読取り線4bに“L”レベルの読取り信号を与えたままとし、他方のフォトダイオード3

１ｂから信号電荷を読み出す時は第２の読取り線４ｂに“Ｈ”レベルの読取り信号を与え、第１の読取り線４ａに“Ｌ”レベルの読取り信号を与えたままとする。

【０１７０】＜第５の実施の形態＞ところで、前記したような２画素／１ユニットの単位セルのアレイを有するＣＭＯＳ固体撮像装置においては、前記したような電子シャッタ機能を持たせない場合でも、２個のフォトダイオード３１ａ、３１ｂから異なるタイミングで信号電荷を読み出す際に前記したようにアドレス線駆動信号を断続的に２回駆動することにより、出力信号を画像表示装置の画面に表示した際の表示画面上の横縞の発生の問題を防止することが可能になる。

【０１７１】図１１は、第５の実施の形態のＣＭＯＳ固体撮像装置における１フィールド期間の一部分の信号読み出し動作の一例を示すタイミング波形図である。

【０１７２】図１１において、φＲＥＳＥＴ、φＡＤＲＥＳ、φＲＥＡＤ１あるいはφＲＥＡＤ２は、パルスセレクタから選択画素行に供給されるパルス信号であり、それぞれ信号読み出し動作の際に水平帰線期間内に活性化されるが、φＲＥＡＤ１、φＲＥＡＤ２は異なる水平帰線期間内に供給される。

【０１７３】ここで、φＲＥＡＤ１が供給される第１の読取り線４ａとアドレス線６との距離よりも、φＲＥＡＤ２が供給される第２の読取り線４ｂとアドレス線６との距離が短く、第１の読取り線４ａとアドレス線６との結合容量よりも第２の読取り線４ｂとアドレス線６との結合容量が大きいので、２個のフォトダイオード３１ａ、３１ｂからそれぞれ読み出される信号電荷に対する影響が異なることに起因して、出力信号を画像表示装置の画面に表示した際の表示画面上の横縞が発生するおそれがある。

【０１７４】しかし、φＡＤＲＥＳは、信号読み出し動作の際の水平帰線期間内に同一行のアドレス線６を２回選択制御するように、断続的に２回活性状態になるように生成され、２個のフォトダイオード３１ａ、３１ｂからそれぞれ信号電荷を読み出す時にφＡＤＲＥＳがそれぞれ“Ｌ”レベルになっているので、上記信号電荷読み出し時の影響がほぼ等しくなり、前記したような表示画面上の横縞の発生の問題を防止できる。

【０１７５】また、本発明は、上記各実施の形態のタイプの固体撮像装置に限らず、光電変換部を積層した積層型の固体撮像装置にも適用可能である。

【０１７６】

【発明の効果】請求項１およびそれに従属する各請求項の固体撮像装置によれば、電子シャッター動作を行わせる場合に読み出し用垂直シフトレジスタと電子シャッタ用垂直シフトレジスタの負荷の変動を防止でき、出力信号の表示画面に発生する横筋の画像ノイズを抑制でき、Ｓ／Ｎの高い鮮明な画像を得ることができる。

【０１７７】請求項３およびそれに従属する各請求項の固体撮像装置によれば、２個の電子シャッタ専用のシフトレジスタにフィールド単位で交互に電子シャッタ動作を振り分けることにより、フィールド単位で信号蓄積時間を変化させる可変電子シャッタ動作（連続電子シャッタ動作）を実現できる。この場合、信号蓄積時間の長短に応じて画素行間に信号蓄積時間の差が生じることを防止でき、出力信号の表示画面における横筋などの画像ノイズの発生を防止することができる。

【０１７８】特に請求項４の固体撮像装置によれば、請求項３の固体撮像装置と同様に連続電子シャッタ動作を実現できるとともに、２個の電子シャッタ専用の垂直シフトレジスタに対応して２本のダミー画素行を設け、読み出し用のシフトレジスタ、２個の電子シャッタ専用のシフトレジスタにより選択制御される３本の画素行を常に選択駆動することにより、画素行選択に伴う負荷の変動をなくし、表示画面上の横筋の発生を防止できる。

【０１７９】請求項１０およびそれに従属する各請求項の固体撮像装置によれば、電子シャッタ動作を実現できるほか、フォトダイオードに隣接する読み出しゲート以外の周辺配線の印加電圧を、信号読み出し動作時の読み出しパルス信号の活性化期間と電子シャッタ動作時の読み出しパルス信号の活性化期間の両方で同じ電圧とし、配線との容量結合によるフォトダイオードからの余分な電荷の読み出しを抑制することにより、黒つぶれのない再生像が得られる。

【０１８０】請求項１２およびそれに従属する請求項の固体撮像装置によれば、撮像領域の２画素／１ユニットの単位セルにおける２画素の光電変換素子からそれぞれ蓄積電荷を読み出す際、この読み出しを制御する配線に隣接し、前記光電変換素子の周辺に存在する他の配線の電圧を、各画素の読み出し時に実質的に同一にするので、２画素の光電変換素子からそれぞれ信号電荷を読み出す時に他の配線の電圧が及ぼす影響がほぼ等しくなり、表示画面上の横縞の発生の問題を防止できる。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態のＣＭＯＳ固体撮像装置の等価回路を示す図。

【図２】本発明の第２の実施の形態のＣＭＯＳ固体撮像装置の等価回路を示す図。

【図３】図２の固体撮像装置において２個の電子シャッタ用垂直シフトレジスタがフィールド単位で交互に電子シャッタ動作を制御する様子を示すタイミング図。

【図４】本発明の第３の実施の形態のＣＭＯＳ固体撮像装置の等価回路を示す図。

【図５】図４中のパルスセレクタの一例を示す回路図。

【図６】図４中のタイミング発生回路、第１の垂直シフトレジスタ～第３の垂直シフトレジスタおよびパルスセレクタの動作例を示すタイミング波形図。

【図７】図６中の１フィールド期間内の電子シャッタ動作の一例を示すタイミング波形図である。

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【図８】図７に示す電子シャッタ動作においてノイズの飛び込みを抑制する動作を説明するために撮像領域の単位セルの一部について示す平面図、断面図および基板内の電位ポテンシャルを示す図。

【図９】本発明の第４の実施の形態の増幅型ＣＭＯＳ固体撮像装置における２画素／１ユニットの単位セルの等価回路を示す図。

【図１０】図９の２画素／１ユニットの単位セルの平面パターンの一例およびその断面構造の一例を概略的に示す図。

【図１１】本発明の第５の実施の形態のＣＭＯＳ固体撮像装置における１フィールド期間内の信号読み出し動作の一例を示すタイミング波形図。

【図１２】従来例１のＣＭＯＳ固体撮像装置の等価回路を示す図。

【図１３】図１２のＣＭＯＳ固体撮像装置の動作例を示すタイミング波形図。

【図１４】図１３中のタイミング発生回路、垂直シフトレジスタおよびパルスセレクタの動作例を示すタイミング波形図。

【図１５】従来例２のＣＭＯＳ固体撮像装置の等価回路を示す図。

【図１６】図１５中の２つの垂直シフトレジスタの行選択タイミングの一例を示す図。

【図１７】図１５の固体撮像装置において信号蓄積時間

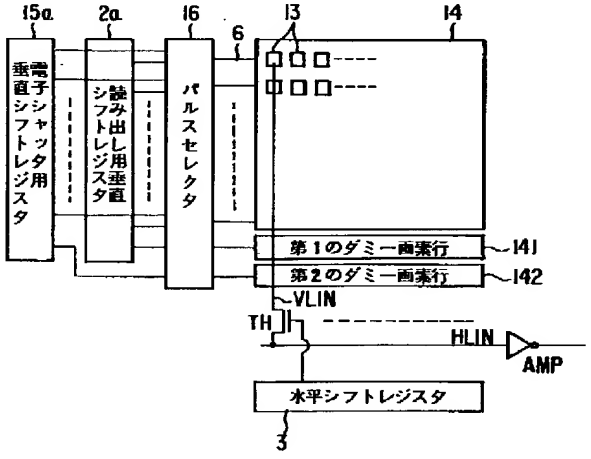
30

を変化させるために、電子シャッタ用垂直シフトレジスタが読み出し用垂直シフトレジスタよりも先に行選択を行うタイミングを変化させて画素信号の蓄積を行う時間の長短を変化させる場合の問題点を説明するために示すタイミング図。

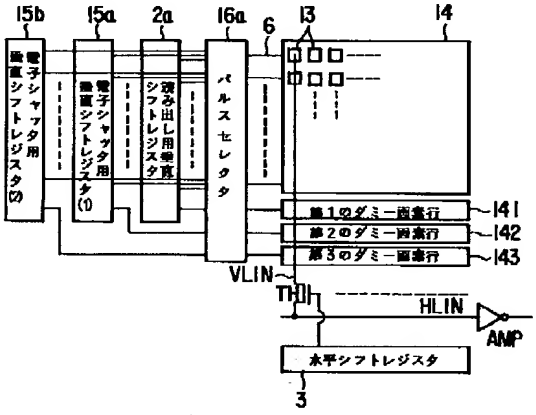
【符号の説明】

２…読み出し用の垂直シフトレジスタ、
３…水平シフトレジスタ、
４…読取り線、
６…垂直選択線、
７…リセット線、
９…電源線、
１０ａ…タイミング発生回路、
２１、２２…電子シャッタ用の垂直シフトレジスタ、
２３…切換制御回路、
２４…垂直駆動回路（パルスセレクタ）、
ＰＤ…フォトダイオード、
Ｔａ…垂直選択トランジスタ（行選択トランジスタ）、
Ｔｂ…増幅トランジスタ、
Ｔｃ…リセットトランジスタ、
Ｔｄ…読み出しトランジスタ、
ＴＨ…水平選択トランジスタ、
VLIN…垂直信号線、
HLIN…水平信号線。

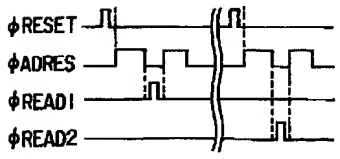
【図１】



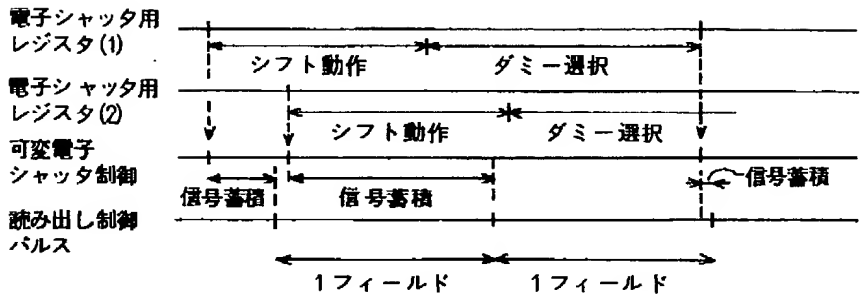
【図２】



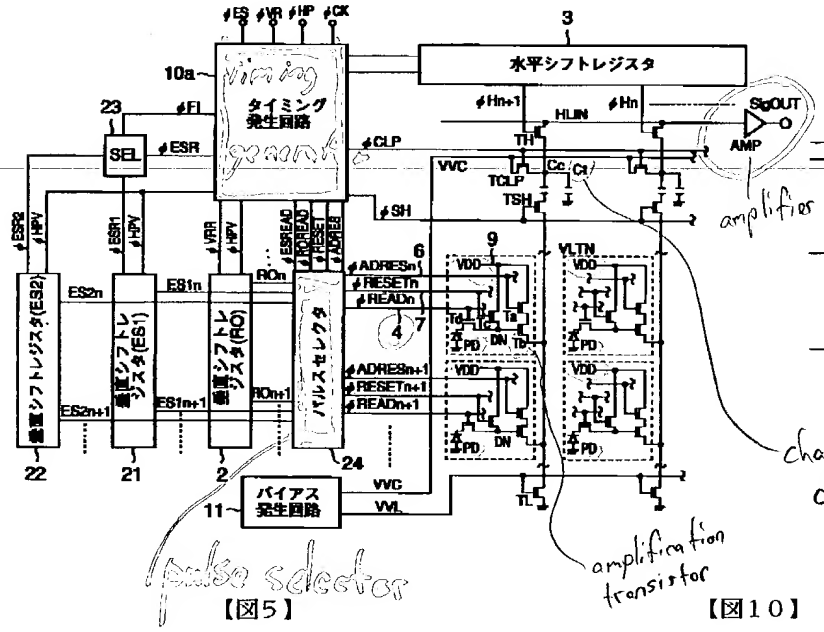
【図１１】



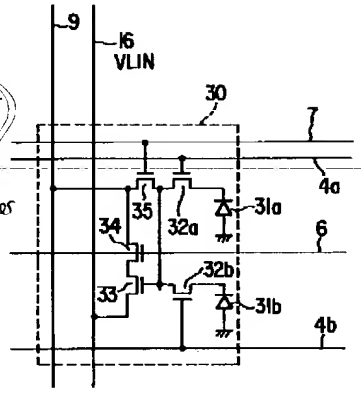
【図3】



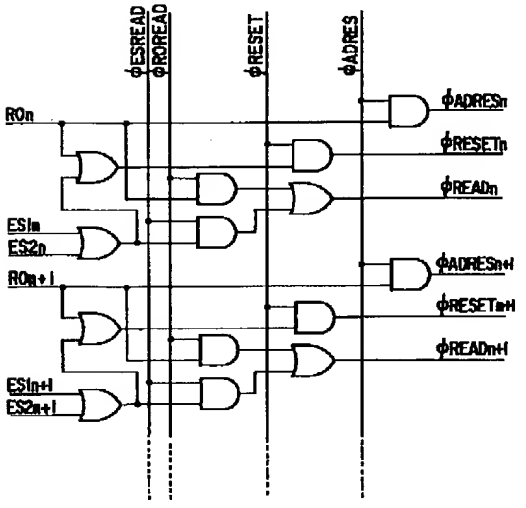
【図4】



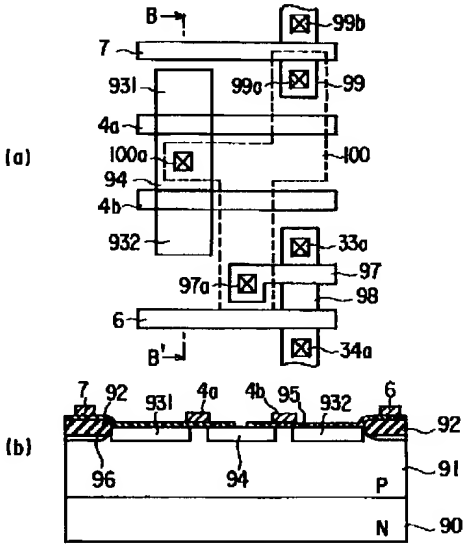
【図9】



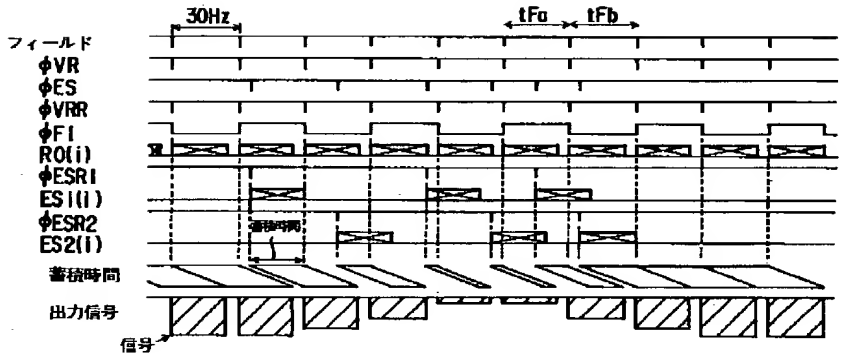
【図5】



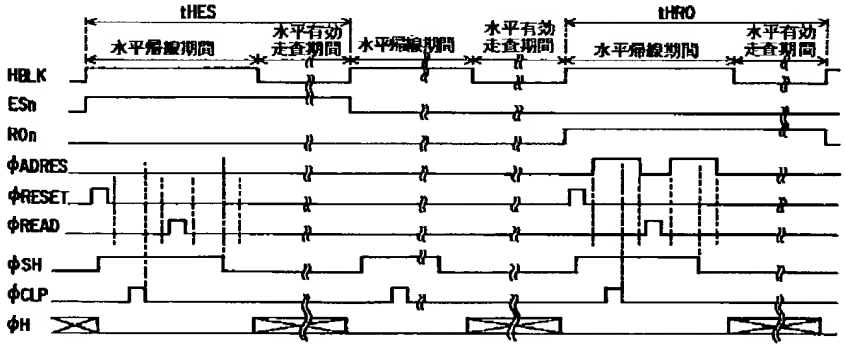
【図10】



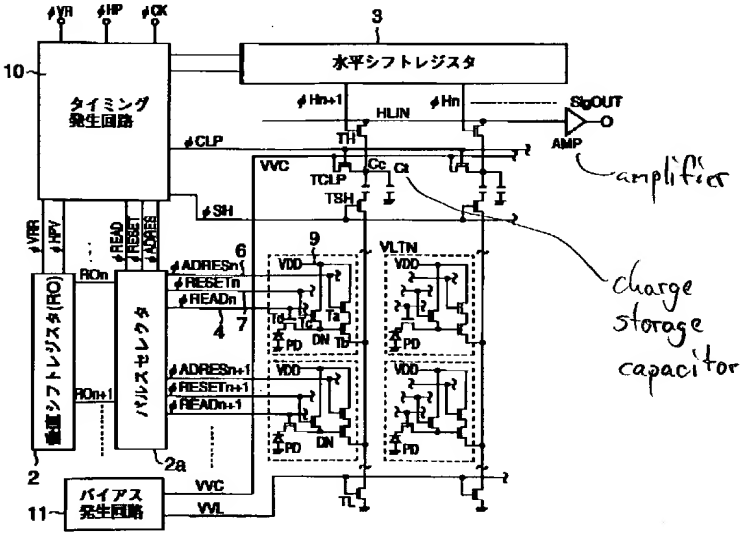
【図6】


30Hz
tFa
tFb
フィールド
φVR
φES
φVRR
φF1
RO(i)
φESR1
ES1(i)
φESR2
ES2(i)
蓄積時間
出力信号
信号

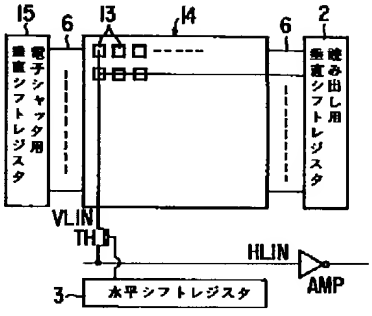
【図7】


tHES
tHRO
水平帰線期間
水平有効走査期間
水平帰線期間
水平有効走査期間
水平帰線期間
水平有効走査期間
HBLK
ESn
ROn
φADRES
φRESET
φREAD
φSH
φCLP
φH

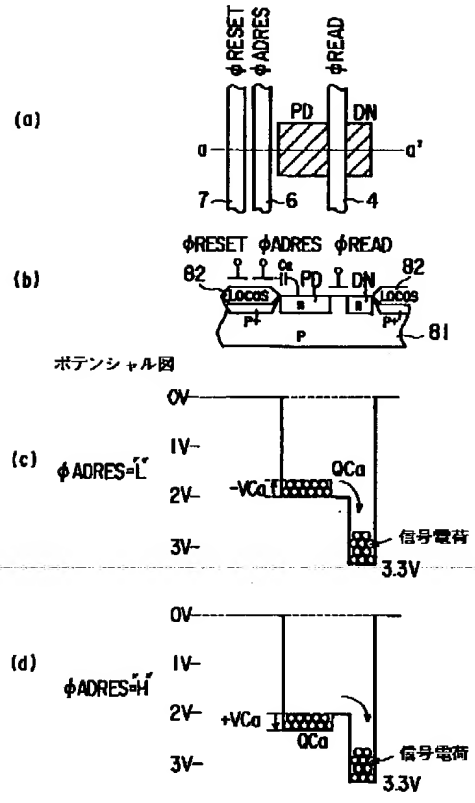
【図12】


φVR
φHP
φCK
3
水平シフトレジスタ
10
タイミング発生回路
φHn+1
φHn
HLIN
SigOUT
AMP
amplifier
φCLP
TH
VVC
TCLP
Cc
Ci
TSH
φSH
charge storage capacitor
φVRR
φHPV
φREAD
φRESET
φADRES
6
9
VLTN
φADRESn
φRESETn
φREADn
4
7
VDD
Tc
Ta
Tb
PD
DN
TL
ROn
ROn+1
垂直シフトレジスタ(RO)
パルスセレクタ
φADRESn+1
φRESETn+1
φREADn+1
2a
2
11
バイアス発生回路
VVC
VVL

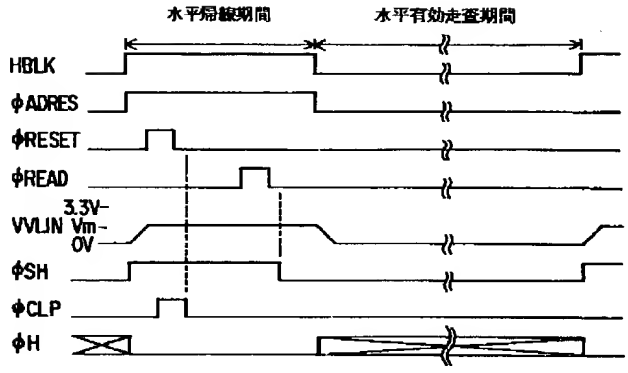
【図15】


15
6
13
14
6
2
垂直シフトレジスタ
電子シャッタ用
読み出し用
垂直シフトレジスタ
VLIN
TH
HLIN
AMP
3
水平シフトレジスタ

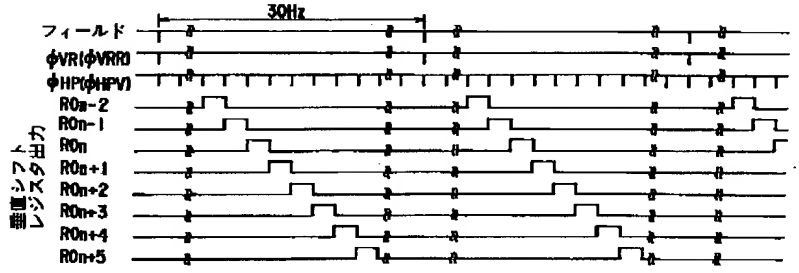
【図8】



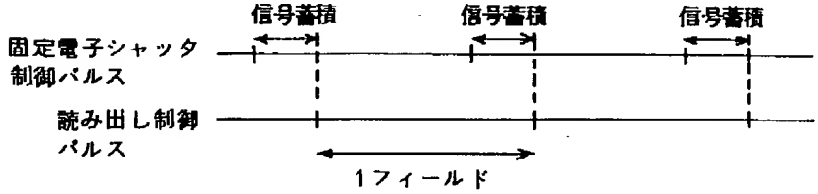
【図13】



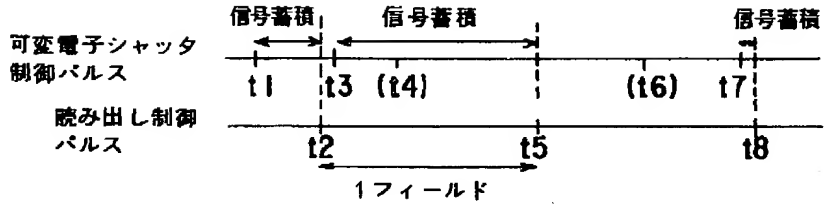
【図14】



【図16】



【図17】



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